In the next few sections we demonstrate the impact of the models of Table 2.1 on the analysis of diode configurations. For those situations where the approximate equivalent circuit will be employed, the diode symbol will appear as shown in Fig. 2.9a for the silicon and germanium diodes. If conditions are such that the ideal diode model can be employed, the diode symbol will appear as shown in Fig. 2.9b.

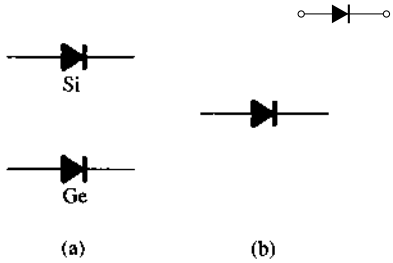

Figure 2.9 (a) Approximate model notation; (b) ideal diode notation.

2.4 SERIES DIODE CONFIGURATIONS WITH DC INPUTS

In this section the approximate model is utilized to investigate a number of series diode configurations with dc inputs. The content will establish a foundation in diode analysis that will carry over into the sections and chapters to follow. The procedure described can, in fact, be applied to networks with any number of diodes in a variety of configurations.

For each configuration the state of each diode must first be determined. Which diodes are "on" and which are "off"? Once determined, the appropriate equivalent as defined in Section 2.3 can be substituted and the remaining parameters of the network determined.

In general, a diode is in the "on" state if the current established by the applied sources is such that its direction matches that of the arrow in the diode symbol, and $V_D \geq 0.7$ V for silicon and $V_D \geq 0.3$ V for germanium.

For each configuration, *mentally* replace the diodes with resistive elements and note the resulting current direction as established by the applied voltages ("pressure"). If the resulting direction is a "match" with the arrow in the diode symbol, conduction through the diode will occur and the device is in the "on" state. The description above is, of course, contingent on the supply having a voltage greater than the "turn-on" voltage (V_T) of each diode.

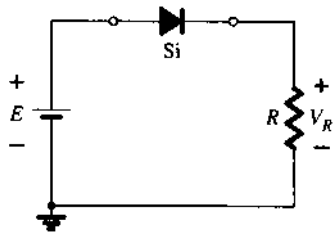

Figure 2.10 Series diode configuration.

If a diode is in the "on" state, one can either place a 0.7-V drop across the element, or the network can be redrawn with the V_T equivalent circuit as defined in Table 2.1. In time the preference will probably simply be to include the 0.7-V drop across each "on" diode and draw a line through each diode in the "off" or open state. Initially, however, the substitution method will be utilized to ensure that the proper voltage and current levels are determined.

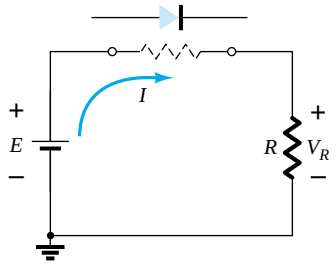

Figure 2.11 Determining the state of the diode of Fig. 2.10.

The series circuit of Fig. 2.10 described in some detail in Section 2.2 will be used to demonstrate the approach described in the paragraphs above. The state of the diode is first determined by mentally replacing the diode with a resistive element as shown in Fig. 2.11. The resulting direction of I is a match with the arrow in the diode symbol, and since $E > V_T$ the diode is in the "on" state. The network is then redrawn as shown in Fig. 2.12 with the appropriate equivalent model for the forward-biased silicon diode. Note for future reference that the polarity of V_D is the same as would result if in fact the diode were a resistive element. The resulting voltage and current levels are the following:

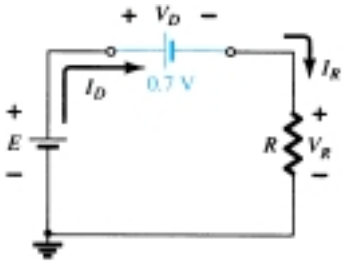

Figure 2.12 Substituting the equivalent model for the "on" diode of Fig. 2.10.

$$V_D = V_T \tag{2.4}$$

$$V_R = E - V_T \tag{2.5}$$

$$I_D = I_R = \frac{V_R}{R} \tag{2.6}$$

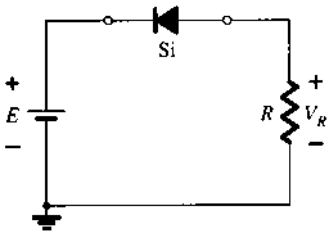

Figure 2.13 Reversing the diode of Fig. 2.10.

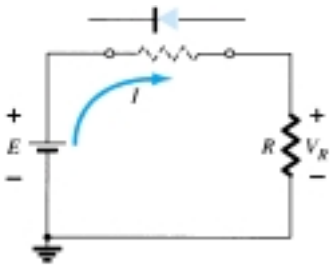

Figure 2.14 Determining the state of the diode of Fig. 2.13.

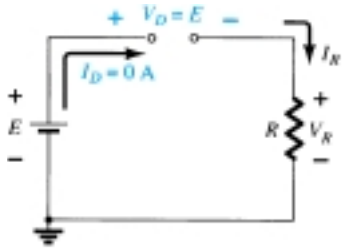

Figure 2.15 Substituting the equivalent model for the "off" diode of Figure 2.13.

In Fig. 2.13 the diode of Fig. 2.10 has been reversed. Mentally replacing the diode with a resistive element as shown in Fig. 2.14 will reveal that the resulting current direction does not match the arrow in the diode symbol. The diode is in the "off" state, resulting in the equivalent circuit of Fig. 2.15. Due to the open circuit, the diode current is 0 A and the voltage across the resistor R is the following:

$$V_R = I_R R = I_D R = (0\text{ A})R = \mathbf{0\text{ V}}$$

The fact that $V_R = 0$ V will establish E volts across the open circuit as defined by Kirchhoff's voltage law. Always keep in mind that under any circumstances—dc, ac instantaneous values, pulses, and so on—Kirchhoff's voltage law must be satisfied!

EXAMPLE 2.6

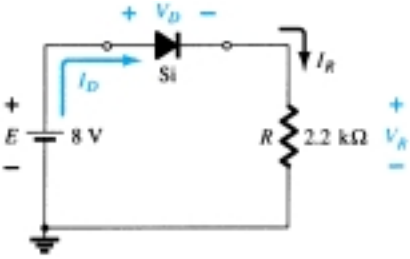

Figure 2.16 Circuit for Example 2.6.

For the series diode configuration of Fig. 2.16, determine V_D, V_R, and I_D.

Solution

Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state,

$$V_D = \mathbf{0.7\text{ V}}$$

$$V_R = E - V_D = 8\text{ V} - 0.7\text{ V} = \mathbf{7.3\text{ V}}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3\text{ V}}{2.2\text{ k}\Omega} \cong \mathbf{3.32\text{ mA}}$$

EXAMPLE 2.7

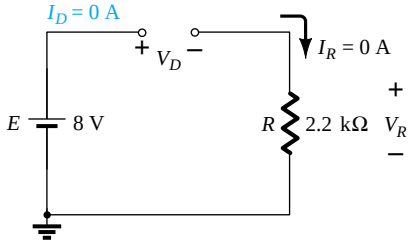

Figure 2.17 Determining the unknown quantities for Example 2.7.

Repeat Example 2.6 with the diode reversed.

Solution

Removing the diode, we find that the direction of I is opposite to the arrow in the diode symbol and the diode equivalent is the open circuit no matter which model is employed. The result is the network of Fig. 2.17, where $I_D = \mathbf{0\text{ A}}$ due to the open circuit. Since $V_R = I_R R$, $V_R = (0)R = 0$ V. Applying Kirchhoff's voltage law around the closed loop yields

$$E - V_D - V_R = 0$$

and

$$V_D = E - V_R = E - 0 = E = \mathbf{8\text{ V}}$$

In particular, note in Example 2.7 the high voltage across the diode even though it is an "off" state. The current is zero, but the voltage is significant. For review purposes, keep the following in mind for the analysis to follow:

1. An open circuit can have any voltage across its terminals, but the current is always 0 A.
2. A short circuit has a 0-V drop across its terminals, but the current is limited only by the surrounding network.

In the next example the notation of Fig. 2.18 will be employed for the applied voltage. It is a common industry notation and one with which the reader should become very familiar. Such notation and other defined voltage levels are treated further in Chapter 4.

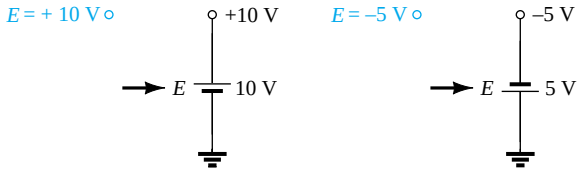

Figure 2.18 Source notation.

EXAMPLE 2.8

For the series diode configuration of Fig. 2.19, determine V_D, V_R, and I_D.

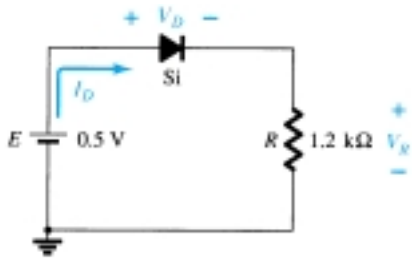

Figure 2.19 Series diode circuit for Example 2.8.

Solution

Although the "pressure" establishes a current with the same direction as the arrow symbol, the level of applied voltage is insufficient to turn the silicon diode "on." The point of operation on the characteristics is shown in Fig. 2.20, establishing the open-circuit equivalent as the appropriate approximation. The resulting voltage and current levels are therefore the following:

$$I_D = \mathbf{0\ A}$$

$$V_R = I_R R = I_D R = (0\ \text{A})1.2\ \text{k}\Omega = \mathbf{0\ V}$$

and

$$V_D = E = \mathbf{0.5\ V}$$

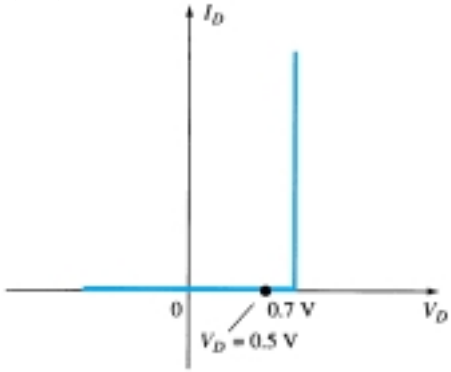

Figure 2.20 Operating point with $E = 0.5$ V.

EXAMPLE 2.9

Determine V_o and I_D for the series circuit of Fig. 2.21.

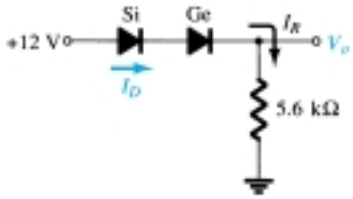

Figure 2.21 Circuit for Example 2.9.

Solution

An attack similar to that applied in Example 2.6 will reveal that the resulting current has the same direction as the arrowheads of the symbols of both diodes, and the network of Fig. 2.22 results because $E = 12\text{ V} > (0.7\text{ V} + 0.3\text{ V}) = 1\text{ V}$. Note the redrawn supply of 12 V and the polarity of V_o across the 5.6-kΩ resistor. The resulting voltage

$$V_o = E - V_{T_1} - V_{T_2} = 12\text{ V} - 0.7\text{ V} - 0.3\text{ V} = \mathbf{11\text{ V}}$$

and

$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{11\text{ V}}{5.6\text{ k}\Omega} \cong \mathbf{1.96\text{ mA}}$$

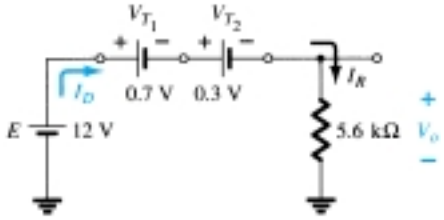

Figure 2.22 Determining the unknown quantities for Example 2.9.

EXAMPLE 2.10

Determine I_D, V_{D_2}, and V_o for the circuit of Fig. 2.23.

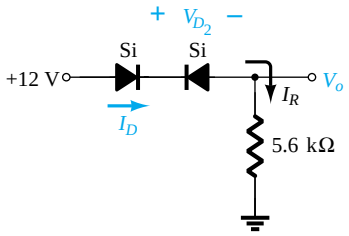

Figure 2.23 Circuit for Example 2.10.

Solution

Removing the diodes and determining the direction of the resulting current I will result in the circuit of Fig. 2.24. There is a match in current direction for the silicon diode but not for the germanium diode. The combination of a short circuit in series with an open circuit always results in an open circuit and $I_D = \mathbf{0\text{ A}}$, as shown in Fig. 2.25.

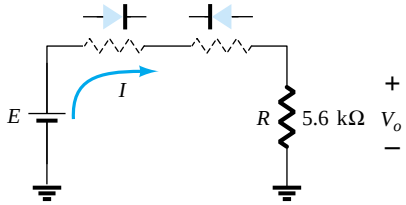

Figure 2.24 Determining the state of the diodes of Figure 2.23.

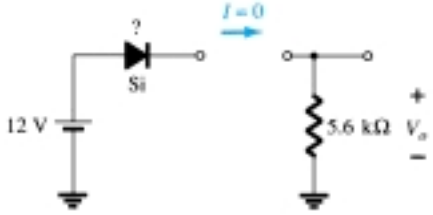

Figure 2.25 Substituting the equivalent state for the open diode.

The question remains as to what to substitute for the silicon diode. For the analysis to follow in this and succeeding chapters, simply recall for the actual practical diode that when $I_D = 0$ A, $V_D = 0$ V (and vice versa), as described for the no-bias situation in Chapter 1. The conditions described by $I_D = 0$ A and $V_{D_1} = 0$ V are indicated in Fig. 2.26.

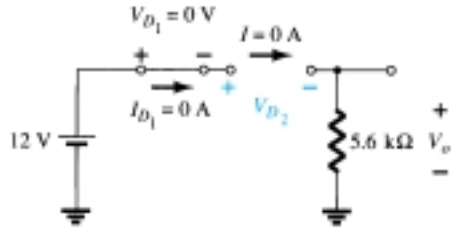

Figure 2.26 Determining the unknown quantities for the circuit of Example 2.10.

$$V_o = I_R R = I_D R = (0 \text{ A})R = 0 \text{ V}$$

and $$V_{D_2} = V_{\text{open circuit}} = E = \mathbf{12\ V}$$

Applying Kirchhoff's voltage law in a clockwise direction gives us

$$E - V_{D_1} - V_{D_2} - V_o = 0$$

and $$V_{D_2} = E - V_{D_1} - V_o = 12 \text{ V} - 0 - 0$$
$$= \mathbf{12\ V}$$

with $$V_o = \mathbf{0\ V}$$

Determine I, V_1, V_2, and V_o for the series dc configuration of Fig. 2.27. *EXAMPLE 2.11*

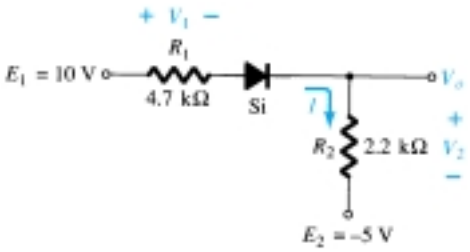

Figure 2.27 Circuit for Example 2.11.

Solution

The sources are drawn and the current direction indicated as shown in Fig. 2.28. The diode is in the "on" state and the notation appearing in Fig. 2.29 is included to indicate this state. Note that the "on" state is noted simply by the additional $V_D = 0.7$ V

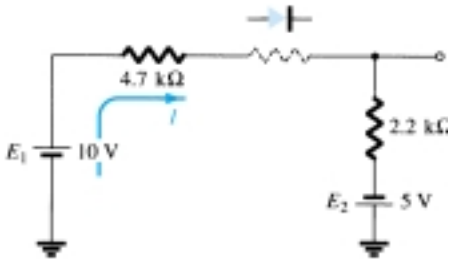

Figure 2.28 Determining the state of the diode for the network of Fig. 2.27.

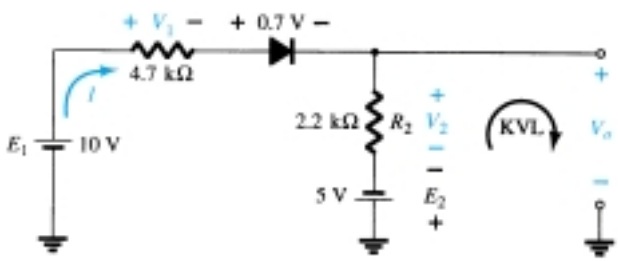

Figure 2.29 Determining the unknown quantities for the network of Fig. 2.27.

on the figure. This eliminates the need to redraw the network and avoids any confusion that may result from the appearance of another source. As indicated in the introduction to this section, this is probably the path and notation that one will take when a level of confidence has been established in the analysis of diode configurations. In time the entire analysis will be performed simply by referring to the original network. Recall that a reverse-biased diode can simply be indicated by a line through the device.

The resulting current through the circuit is,

$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{10\text{ V} + 5\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega} = \frac{14.3\text{ V}}{6.9\text{ k}\Omega}$$

$$\cong \mathbf{2.072\text{ mA}}$$

and the voltages are

$$V_1 = IR_1 = (2.072\text{ mA})(4.7\text{ k}\Omega) = \mathbf{9.74\text{ V}}$$

$$V_2 = IR_2 = (2.072\text{ mA})(2.2\text{ k}\Omega) = \mathbf{4.56\text{ V}}$$

Applying Kirchhoff's voltage law to the output section in the clockwise direction will result in

$$-E_2 + V_2 - V_o = 0$$

and

$$V_o = V_2 - E_2 = 4.56\text{ V} - 5\text{ V} = \mathbf{-0.44\text{ V}}$$

The minus sign indicates that V_o has a polarity opposite to that appearing in Fig. 2.27.

2.5 PARALLEL AND SERIES–PARALLEL CONFIGURATIONS

The methods applied in Section 2.4 can be extended to the analysis of parallel and series–parallel configurations. For each area of application, simply match the sequential series of steps applied to series diode configurations.

EXAMPLE 2.12

Determine V_o, I_1, I_{D_1}, and I_{D_2} for the parallel diode configuration of Fig. 2.30.

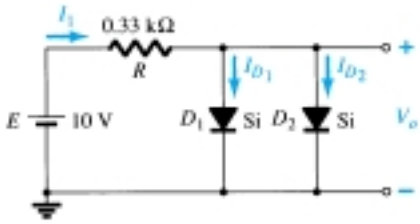

Figure 2.30 Network for Example 2.12.

Solution

For the applied voltage the "pressure" of the source is to establish a current through each diode in the same direction as shown in Fig. 2.31. Since the resulting current direction matches that of the arrow in each diode symbol and the applied voltage is greater than 0.7 V, both diodes are in the "on" state. The voltage across parallel elements is always the same and

$$V_o = \mathbf{0.7\text{ V}}$$

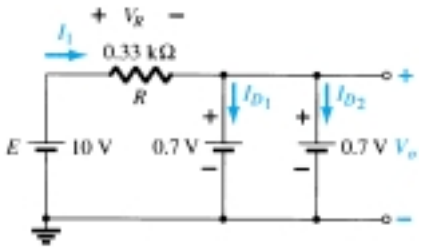

Figure 2.31 Determining the unknown quantities for the network of Example 2.12.

The current

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{0.33\text{ k}\Omega} = \mathbf{28.18\text{ mA}}$$

Assuming diodes of similar characteristics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\text{ mA}}{2} = \mathbf{14.09\text{ mA}}$$

Example 2.12 demonstrated one reason for placing diodes in parallel. If the current rating of the diodes of Fig. 2.30 is only 20 mA, a current of 28.18 mA would damage the device if it appeared alone in Fig. 2.30. By placing two in parallel, the current is limited to a safe value of 14.09 mA with the same terminal voltage.

EXAMPLE 2.13

Determine the current I for the network of Fig. 2.32.

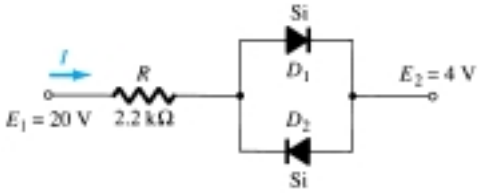

Figure 2.32 Network for Example 2.13.

Solution

Redrawing the network as shown in Fig. 2.33 reveals that the resulting current direction is such as to turn on diode D_1 and turn off diode D_2. The resulting current I is then

$$I = \frac{E_1 - E_2 - V_D}{R} = \frac{20\text{ V} - 4\text{ V} - 0.7\text{ V}}{2.2\text{ k}\Omega} \cong \mathbf{6.95\text{ mA}}$$

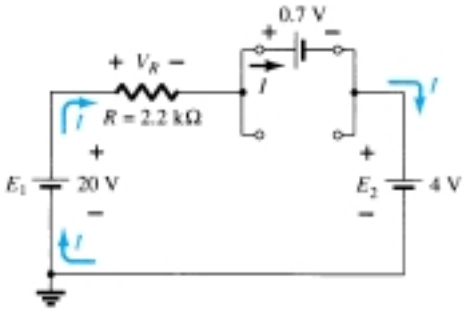

Figure 2.33 Determining the unknown quantities for the network of Example 2.13.

EXAMPLE 2.14

Determine the voltage V_o for the network of Fig. 2.34.

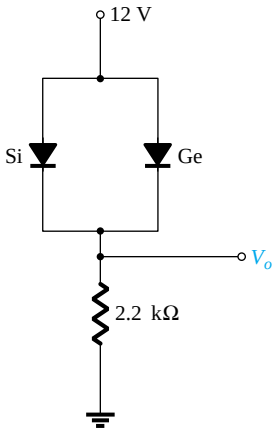

Figure 2.34 Network for Example 2.14.

Solution

Initially, it would appear that the applied voltage will turn both diodes "on." However, if both were "on," the 0.7-V drop across the silicon diode would not match the 0.3 V across the germanium diode as required by the fact that the voltage across parallel elements must be the same. The resulting action can be explained simply by realizing that when the supply is turned on it will increase from 0 to 12 V over a period of time—although probably measurable in milliseconds. At the instant during the rise that 0.3 V is established across the germanium diode it will turn "on" and maintain a level of 0.3 V. The silicon diode will never have the opportunity to capture its required 0.7 V and therefore remains in its open-circuit state as shown in Fig. 2.35. The result:

$$V_o = 12\text{ V} - 0.3\text{ V} = \mathbf{11.7\text{ V}}$$

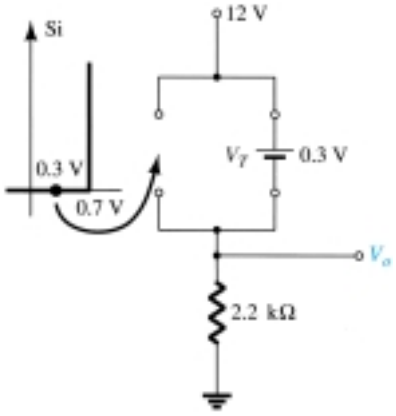

Figure 2.35 Determining V_o for the network of Fig. 2.34.

EXAMPLE 2.15

Determine the currents I_1, I_2, and I_{D_2} for the network of Fig. 2.36.

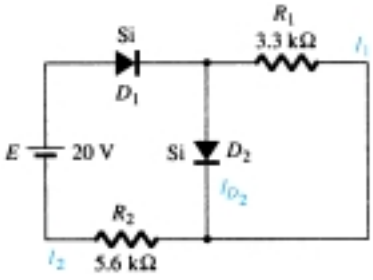

Figure 2.36 Network for Example 2.15.

Solution

The applied voltage (pressure) is such as to turn both diodes on, as noted by the resulting current directions in the network of Fig. 2.37. Note the use of the abbreviated notation for "on" diodes and that the solution is obtained through an application of techniques applied to dc series—parallel networks.

$$I_1 = \frac{V_{T_2}}{R_1} = \frac{0.7\text{ V}}{3.3\text{ k}\Omega} = \mathbf{0.212\text{ mA}}$$

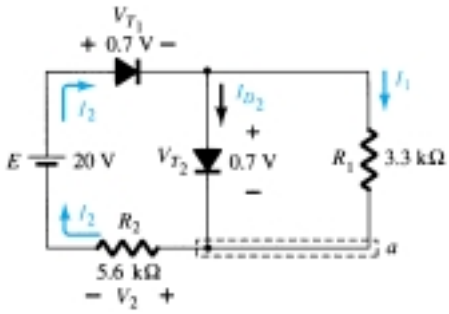

Figure 2.37 Determining the unknown quantities for Example 2.15.

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction yields

$$-V_2 + E - V_{T_1} - V_{T_2} = 0$$

and $$V_2 = E - V_{T_1} - V_{T_2} = 20\text{ V} - 0.7\text{ V} - 0.7\text{ V} = 18.6\text{ V}$$

with $$I_2 = \frac{V_2}{R_2} = \frac{18.6\text{ V}}{5.6\text{ k}\Omega} = \mathbf{3.32\text{ mA}}$$

At the bottom node (a),

$$I_{D_2} + I_1 = I_2$$

and $$I_{D_2} = I_2 - I_1 = 3.32\text{ mA} - 0.212\text{ mA} = \mathbf{3.108\text{ mA}}$$

2.6 AND/OR GATES

The tools of analysis are now at our disposal, and the opportunity to investigate a computer configuration is one that will demonstrate the range of applications of this relatively simple device. Our analysis will be limited to determining the voltage levels and will not include a detailed discussion of Boolean algebra or positive and negative logic.

The network to be analyzed in Example 2.16 is an OR gate for positive logic. That is, the 10-V level of Fig. 2.38 is assigned a "1" for Boolean algebra while the 0-V input is assigned a "0." An OR gate is such that the output voltage level will be a 1 if either *or* both inputs is a 1. The output is a 0 if both inputs are at the 0 level.

The analysis of AND/OR gates is made measurably easier by using the approximate equivalent for a diode rather than the ideal because we can stipulate that the voltage across the diode must be 0.7 V positive for the silicon diode (0.3 V for Ge) to switch to the "on" state.

In general, the best approach is simply to establish a "gut" feeling for the state of the diodes by noting the direction and the "pressure" established by the applied potentials. The analysis will then verify or negate your initial assumptions.

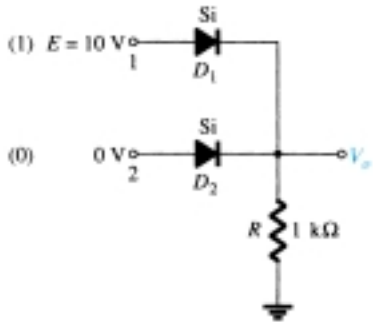

Figure 2.38 Positive logic OR gate.

EXAMPLE 2.16

Determine V_o for the network of Fig. 2.38.

Solution

First note that there is only one applied potential; 10 V at terminal 1. Terminal 2 with a 0-V input is essentially at ground potential, as shown in the redrawn network of Fig. 2.39. Figure 2.39 "suggests" that D_1 is probably in the "on" state due to the applied 10 V while D_2 with its "positive" side at 0 V is probably "off." Assuming these states will result in the configuration of Fig. 2.40.

The next step is simply to check that there is no contradiction to our assumptions. That is, note that the polarity across D_1 is such as to turn it on and the polarity across D_2 is such as to turn it off. For D_1 the "on" state establishes V_o at $V_o = E - V_D = 10\text{ V} - 0.7\text{ V} = \mathbf{9.3\text{ V}}$. With 9.3 V at the cathode (−) side of D_2 and 0 V at the anode (+) side, D_2 is definitely in the "off" state. The current direction and the resulting continuous path for conduction further confirm our assumption that D_1 is conducting. Our assumptions seem confirmed by the resulting voltages and current, and our initial analysis can be assumed to be correct. The output voltage level is not 10 V as defined for an input of 1, but the 9.3 V is sufficiently large to be considered a 1 level. The output is therefore at a 1 level with only one input, which suggests that

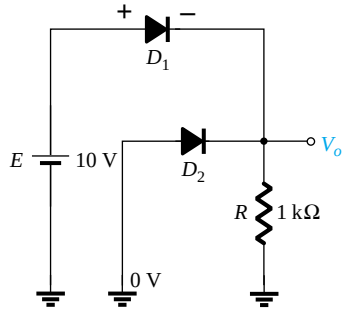

Figure 2.39 Redrawn network of Fig. 2.38.