Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction yields

$$-V_2 + E - V_{T_1} - V_{T_2} = 0$$

and $$V_2 = E - V_{T_1} - V_{T_2} = 20\text{ V} - 0.7\text{ V} - 0.7\text{ V} = 18.6\text{ V}$$

with $$I_2 = \frac{V_2}{R_2} = \frac{18.6\text{ V}}{5.6\text{ k}\Omega} = \mathbf{3.32\text{ mA}}$$

At the bottom node (a),

$$I_{D_2} + I_1 = I_2$$

and $$I_{D_2} = I_2 - I_1 = 3.32\text{ mA} - 0.212\text{ mA} = \mathbf{3.108\text{ mA}}$$

2.6 AND/OR GATES

The tools of analysis are now at our disposal, and the opportunity to investigate a computer configuration is one that will demonstrate the range of applications of this relatively simple device. Our analysis will be limited to determining the voltage levels and will not include a detailed discussion of Boolean algebra or positive and negative logic.

The network to be analyzed in Example 2.16 is an OR gate for positive logic. That is, the 10-V level of Fig. 2.38 is assigned a "1" for Boolean algebra while the 0-V input is assigned a "0." An OR gate is such that the output voltage level will be a 1 if either *or* both inputs is a 1. The output is a 0 if both inputs are at the 0 level.

The analysis of AND/OR gates is made measurably easier by using the approximate equivalent for a diode rather than the ideal because we can stipulate that the voltage across the diode must be 0.7 V positive for the silicon diode (0.3 V for Ge) to switch to the "on" state.

In general, the best approach is simply to establish a "gut" feeling for the state of the diodes by noting the direction and the "pressure" established by the applied potentials. The analysis will then verify or negate your initial assumptions.

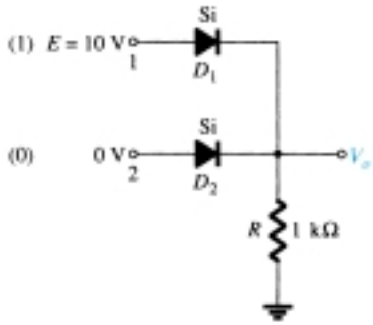

Figure 2.38 Positive logic OR gate.

EXAMPLE 2.16

Determine V_o for the network of Fig. 2.38.

Solution

First note that there is only one applied potential; 10 V at terminal 1. Terminal 2 with a 0-V input is essentially at ground potential, as shown in the redrawn network of Fig. 2.39. Figure 2.39 "suggests" that D_1 is probably in the "on" state due to the applied 10 V while D_2 with its "positive" side at 0 V is probably "off." Assuming these states will result in the configuration of Fig. 2.40.

The next step is simply to check that there is no contradiction to our assumptions. That is, note that the polarity across D_1 is such as to turn it on and the polarity across D_2 is such as to turn it off. For D_1 the "on" state establishes V_o at $V_o = E - V_D = 10\text{ V} - 0.7\text{ V} = \mathbf{9.3\text{ V}}$. With 9.3 V at the cathode (−) side of D_2 and 0 V at the anode (+) side, D_2 is definitely in the "off" state. The current direction and the resulting continuous path for conduction further confirm our assumption that D_1 is conducting. Our assumptions seem confirmed by the resulting voltages and current, and our initial analysis can be assumed to be correct. The output voltage level is not 10 V as defined for an input of 1, but the 9.3 V is sufficiently large to be considered a 1 level. The output is therefore at a 1 level with only one input, which suggests that

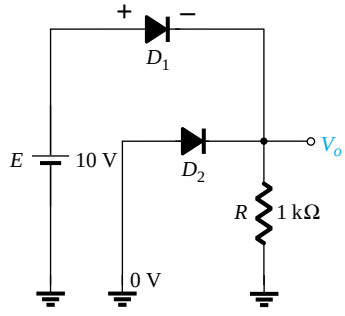

Figure 2.39 Redrawn network of Fig. 2.38.

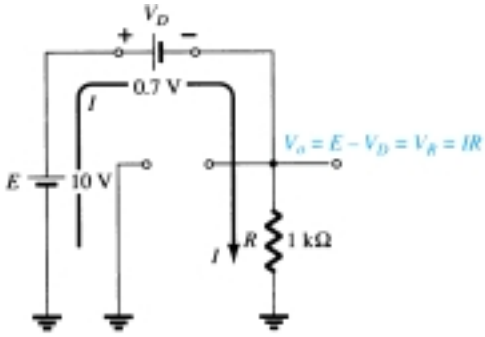

Figure 2.40 Assumed diode states for Fig. 2.38.

the gate is an OR gate. An analysis of the same network with two 10-V inputs will result in both diodes being in the "on" state and an output of 9.3 V. A 0-V input at both inputs will not provide the 0.7 V required to turn the diodes on, and the output will be a 0 due to the 0-V output level. For the network of Fig. 2.40 the current level is determined by

$$I = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

EXAMPLE 2.17

Determine the output level for the positive logic AND gate of Fig. 2.41.

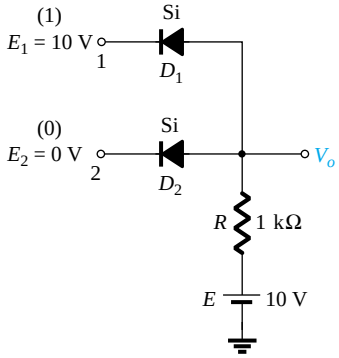

Figure 2.41 Positive logic AND gate.

Solution

Note in this case that an independent source appears in the grounded leg of the network. For reasons soon to become obvious it is chosen at the same level as the input logic level. The network is redrawn in Fig. 2.42 with our initial assumptions regarding the state of the diodes. With 10 V at the cathode side of D_1 it is assumed that D_1 is in the "off" state even though there is a 10-V source connected to the anode of D_1 through the resistor. However, recall that we mentioned in the introduction to this section that the use of the approximate model will be an aid to the analysis. For D_1, where will the 0.7 V come from if the input and source voltages are at the same level and creating opposing "pressures"? D_2 is assumed to be in the "on" state due to the low voltage at the cathode side and the availability of the 10-V source through the 1-kΩ resistor.

For the network of Fig. 2.42 the voltage at V_o is 0.7 V due to the forward-biased diode D_2. With 0.7 V at the anode of D_1 and 10 V at the cathode, D_1 is definitely in the "off" state. The current I will have the direction indicated in Fig. 2.42 and a magnitude equal to

$$I = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

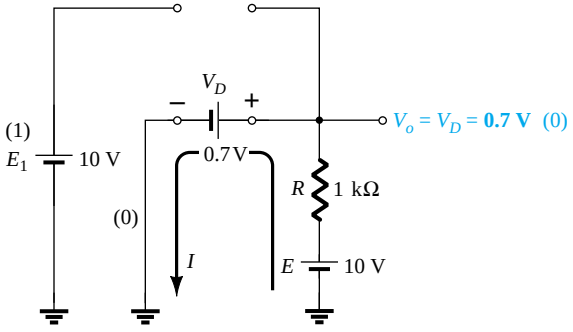

Figure 2.42 Substituting the assumed states for the diodes of Fig. 2.41.

The state of the diodes is therefore confirmed and our earlier analysis was correct. Although not 0 V as earlier defined for the 0 level, the output voltage is sufficiently small to be considered a 0 level. For the AND gate, therefore, a single input will result in a 0-level output. The remaining states of the diodes for the possibilities of two inputs and no inputs will be examined in the problems at the end of the chapter.

2.7 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The diode analysis will now be expanded to include time-varying functions such as the sinusoidal waveform and the square wave. There is no question that the degree of difficulty will increase, but once a few fundamental maneuvers are understood, the analysis will be fairly direct and follow a common thread.

The simplest of networks to examine with a time-varying signal appears in Fig. 2.43. For the moment we will use the ideal model (note the absence of the Si or Ge label to denote ideal diode) to ensure that the approach is not clouded by additional mathematical complexity.

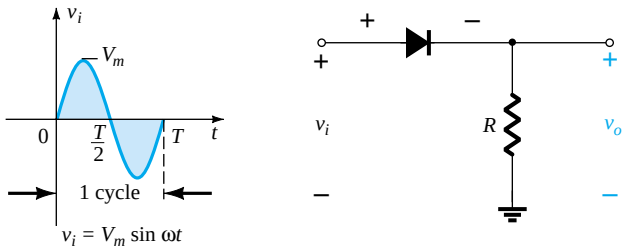

Figure 2.43 Half-wave rectifier.

Over one full cycle, defined by the period T of Fig. 2.43, the average value (the algebraic sum of the areas above and below the axis) is zero. The circuit of Fig. 2.43, called a *half-wave rectifier,* will generate a waveform v_o that will have an average value of particular, use in the ac-to-dc conversion process. When employed in the rectification process, a diode is typically referred to as a *rectifier.* Its power and current ratings are typically much higher than those of diodes employed in other applications, such as computers and communication systems.

During the interval $t = 0 \rightarrow T/2$ in Fig. 2.43 the polarity of the applied voltage v_i is such as to establish "pressure" in the direction indicated and turn on the diode with the polarity appearing above the diode. Substituting the short-circuit equivalence for the ideal diode will result in the equivalent circuit of Fig. 2.44, where it is fairly obvious that the output signal is an exact replica of the applied signal. The two terminals defining the output voltage are connected directly to the applied signal via the short-circuit equivalence of the diode.

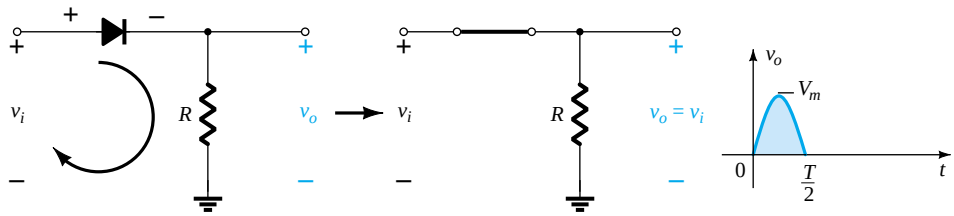

Figure 2.44 Conduction region $(0 \rightarrow T/2)$.

For the period $T/2 \rightarrow T$, the polarity of the input v_i is as shown in Fig. 2.45 and the resulting polarity across the ideal diode produces an "off" state with an open-circuit equivalent. The result is the absence of a path for charge to flow and $v_o = iR = (0)R = 0$ V for the period $T/2 \rightarrow T$. The input v_i and the output v_o were sketched together in Fig. 2.46 for comparison purposes. The output signal v_o now has a net positive area above the axis over a full period and an average value determined by

$$V_{dc} = 0.318V_m \quad \text{half-wave} \tag{2.7}$$

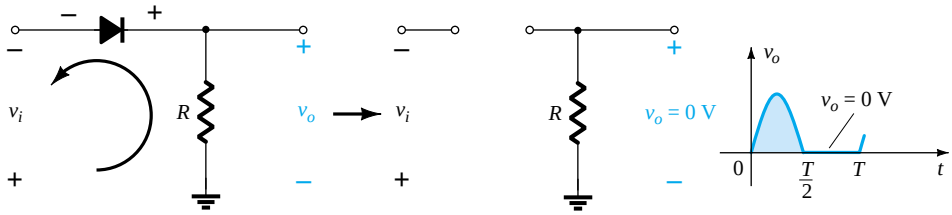

Figure 2.45 Nonconduction region ($T/2 \rightarrow T$).

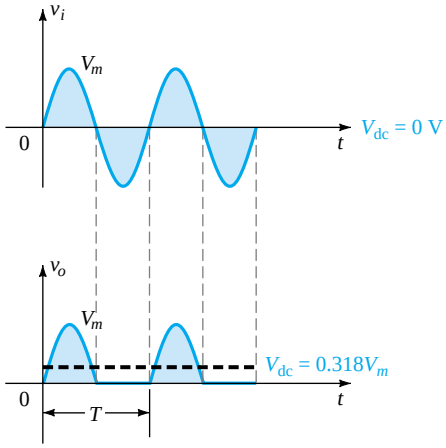

Figure 2.46 Half-wave rectified signal.

The process of removing one-half the input signal to establish a dc level is aptly called *half-wave rectification.*

The effect of using a silicon diode with $V_T = 0.7$ V is demonstrated in Fig. 2.47 for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on." For levels of v_i less than 0.7 V, the diode is still in an open-circuit state and $v_o = 0$ V as shown in the same figure. When conducting, the difference between v_o and v_i is a fixed level of $V_T = 0.7$ V and $v_o = v_i - V_T$, as shown in the figure. The net effect is a reduction in area above the axis, which naturally reduces

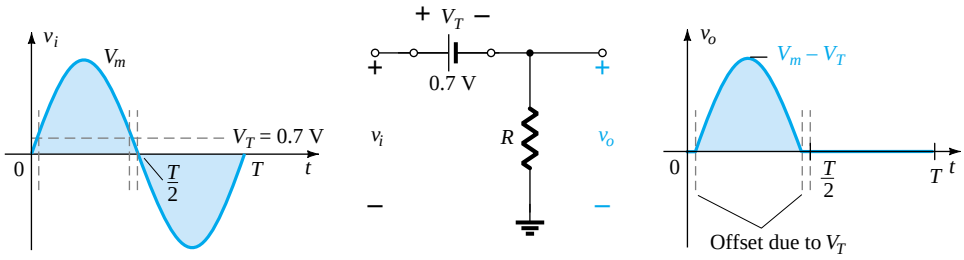

Figure 2.47 Effect of V_T on half-wave rectified signal.

the resulting dc voltage level. For situations where $V_m \gg V_T$, Eq. 2.8 can be applied to determine the average value with a relatively high level of accuracy.

$$V_{dc} \cong 0.318(V_m - V_T) \tag{2.8}$$

In fact, if V_m is sufficiently greater than V_T, Eq. 2.7 is often applied as a first approximation for V_{dc}.

EXAMPLE 2.18

(a) Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.48.
(b) Repeat part (a) if the ideal diode is replaced by a silicon diode.
(c) Repeat parts (a) and (b) if V_m is increased to 200 V and compare solutions using Eqs. (2.7) and (2.8).

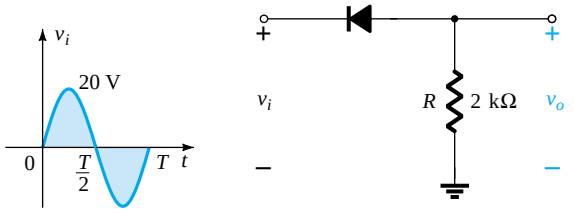

Figure 2.48 Network for Example 2.18.

Solution

(a) In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.49, and v_o will appear as shown in the same figure. For the full period, the dc level is

$$V_{dc} = -0.318V_m = -0.318(20\text{ V}) = \mathbf{-6.36\text{ V}}$$

The negative sign indicates that the polarity of the output is opposite to the defined polarity of Fig. 2.48.

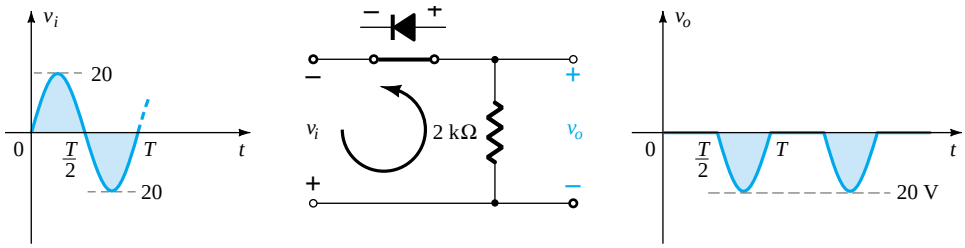

Figure 2.49 Resulting v_o for the circuit of Example 2.18.

(b) Using a silicon diode, the output has the appearance of Fig. 2.50 and

$$V_{dc} \cong -0.318(V_m - 0.7\text{ V}) = -0.318(19.3\text{ V}) \cong \mathbf{-6.14\text{ V}}$$

The resulting drop in dc level is 0.22 V or about 3.5%.

(c) Eq. (2.7): $V_{dc} = -0.318V_m = -0.318(200\text{ V}) = \mathbf{-63.6\text{ V}}$

Eq. (2.8): $V_{dc} = -0.318(V_m - V_T) = -0.318(200\text{ V} - 0.7\text{ V})$

$= -(0.318)(199.3\text{ V}) = \mathbf{-63.38\text{ V}}$

which is a difference that can certainly be ignored for most applications. For part c the offset and drop in amplitude due to V_T would not be discernible on a typical oscilloscope if the full pattern is displayed.

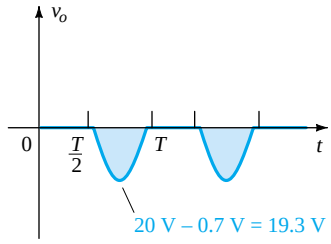

Figure 2.50 Effect of V_T on output of Fig. 2.49.

PIV (PRV)

The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region. The required PIV rating for the half-wave rectifier can be determined from Fig. 2.51, which displays the reverse-biased diode of Fig. 2.43 with maximum applied voltage. Applying Kirchhoff"s voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore,

$$\text{PIV rating} \geqq V_m \quad \text{half-wave rectifier} \tag{2.9}$$

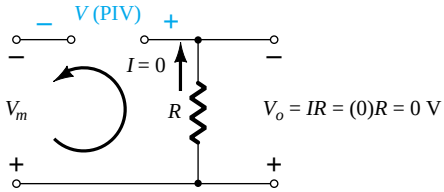

Figure 2.51 Determining the required PIV rating for the half-wave rectifier.

2.8 FULL-WAVE RECTIFICATION

Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification.* The most familiar network for performing such a function appears in Fig. 2.52 with its four diodes in a *bridge* configuration. During the period $t = 0$ to $T/2$ the polarity of the input is as shown in Fig. 2.53. The resulting polarities across the ideal diodes are also shown in Fig. 2.53 to reveal that D_2 and D_3 are conducting while D_1 and D_4 are in the "off" state. The net result is the configuration of Fig. 2.54, with its indicated current and polarity across R. Since the diodes are ideal the load voltage is $v_o = v_i$, as shown in the same figure.

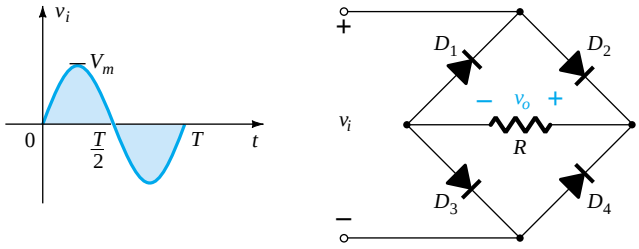

Figure 2.52 Full-wave bridge rectifier.

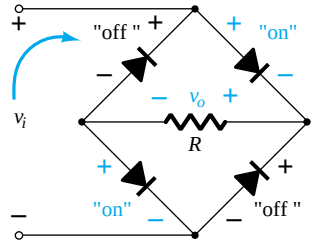

Figure 2.53 Network of Fig. 2.52 for the period $0 \rightarrow T/2$ of the input voltage v_i.

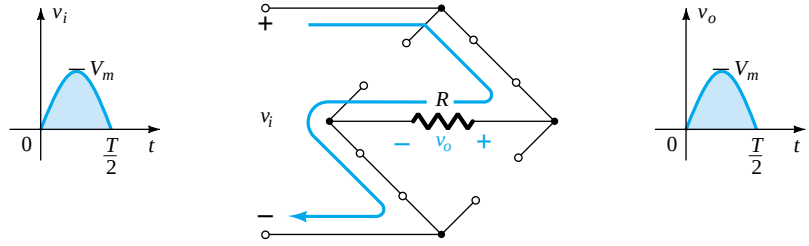

Figure 2.54 Conduction path for the positive region of v_i.