PIV (PRV)

The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region. The required PIV rating for the half-wave rectifier can be determined from Fig. 2.51, which displays the reverse-biased diode of Fig. 2.43 with maximum applied voltage. Applying Kirchhoff"s voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore,

$$\text{PIV rating} \geqq V_m \quad \text{half-wave rectifier} \tag{2.9}$$

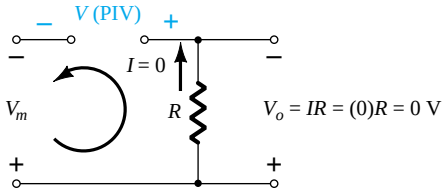

Figure 2.51 Determining the required PIV rating for the half-wave rectifier.

2.8 FULL-WAVE RECTIFICATION

Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification.* The most familiar network for performing such a function appears in Fig. 2.52 with its four diodes in a *bridge* configuration. During the period $t = 0$ to $T/2$ the polarity of the input is as shown in Fig. 2.53. The resulting polarities across the ideal diodes are also shown in Fig. 2.53 to reveal that D_2 and D_3 are conducting while D_1 and D_4 are in the "off" state. The net result is the configuration of Fig. 2.54, with its indicated current and polarity across R. Since the diodes are ideal the load voltage is $v_o = v_i$, as shown in the same figure.

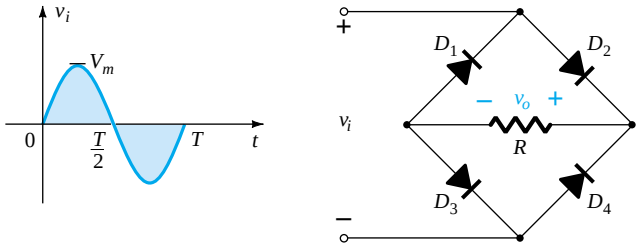

Figure 2.52 Full-wave bridge rectifier.

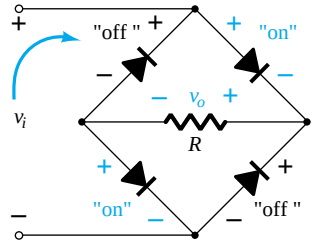

Figure 2.53 Network of Fig. 2.52 for the period $0 \rightarrow T/2$ of the input voltage v_i.

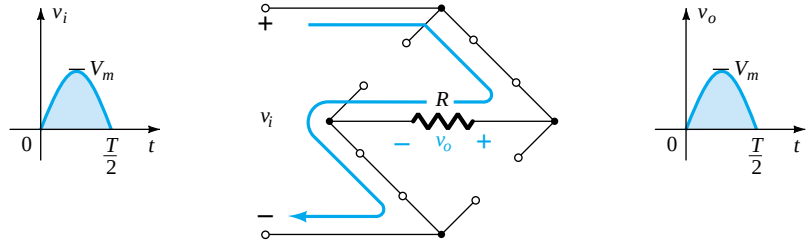

Figure 2.54 Conduction path for the positive region of v_i.

For the negative region of the input the conducting diodes are D_1 and D_4, resulting in the configuration of Fig. 2.55. The important result is that the polarity across the load resistor R is the same as in Fig. 2.53, establishing a second positive pulse, as shown in Fig. 2.55. Over one full cycle the input and output voltages will appear as shown in Fig. 2.56.

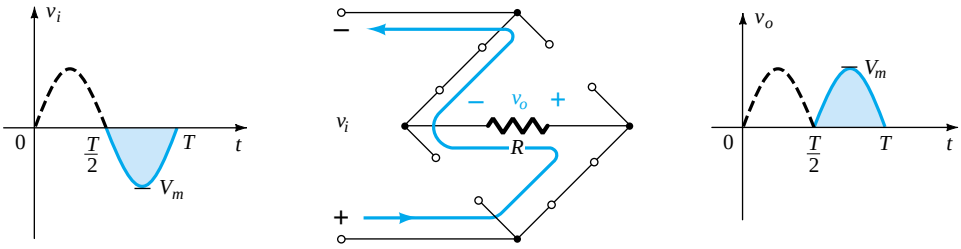

Figure 2.55 Conduction path for the negative region of v_i.

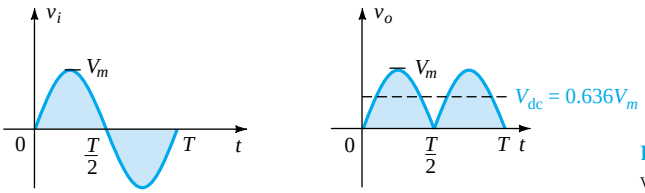

Figure 2.56 Input and output waveforms for a full-wave rectifier.

Since the area above the axis for one full cycle is now twice that obtained for a half-wave system, the dc level has also been doubled and

$$V_{dc} = 2(\text{Eq. } 2.7) = 2(0.318V_m)$$

or

$$\boxed{V_{dc} = 0.636V_m} \quad \text{full-wave} \tag{2.10}$$

If silicon rather than ideal diodes are employed as shown in Fig. 2.57, an application of Kirchhoff's voltage law around the conduction path would result in

$$v_i - V_T - v_o - V_T = 0$$

and

$$v_o = v_i - 2V_T$$

The peak value of the output voltage v_o is therefore

$$V_{o_{max}} = V_m - 2V_T$$

For situations where $V_m \gg 2V_T$, Eq. (2.11) can be applied for the average value with a relatively high level of accuracy.

$$\boxed{V_{dc} \cong 0.636(V_m - 2V_T)} \tag{2.11}$$

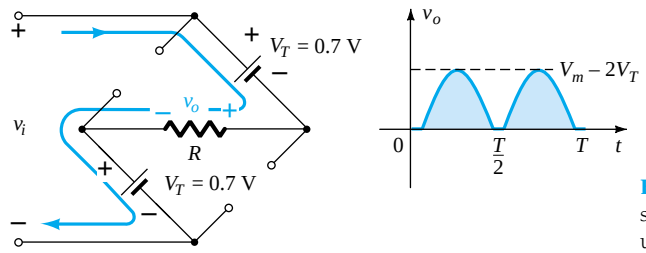

Figure 2.57 Determining $V_{o_{max}}$ for silicon diodes in the bridge configuration.

Then again, if V_m is sufficiently greater than $2V_T$, then Eq. (2.10) is often applied as a first approximation for V_{dc}.

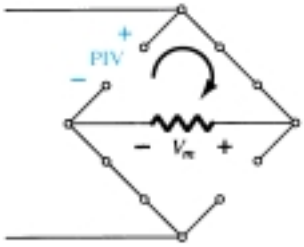

Figure 2.58 Determining the required PIV for the bridge configuration.

PIV

The required PIV of each diode (ideal) can be determined from Fig. 2.58 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across R is V_m and the PIV rating is defined by

$$\text{PIV} \geqq V_m \quad \text{full-wave bridge rectifier} \tag{2.12}$$

Center-Tapped Transformer

A second popular full-wave rectifier appears in Fig. 2.59 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of v_i applied to the primary of the transformer, the network will appear as shown in Fig. 2.60. D_1 assumes the short-circuit equivalent and D_2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as shown in Fig. 2.60.

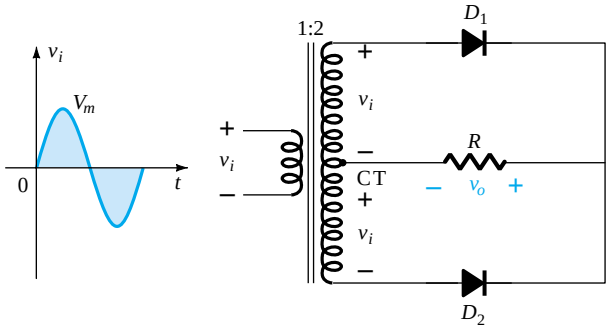

Figure 2.59 Center-tapped transformer full-wave rectifier.

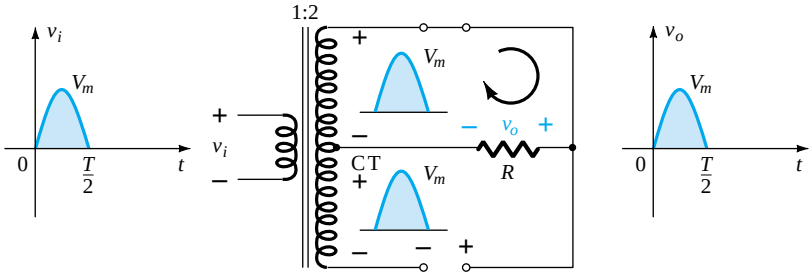

Figure 2.60 Network conditions for the positive region of v_i.

During the negative portion of the input the network appears as shown in Fig. 2.61, reversing the roles of the diodes but maintaining the same polarity for the volt-

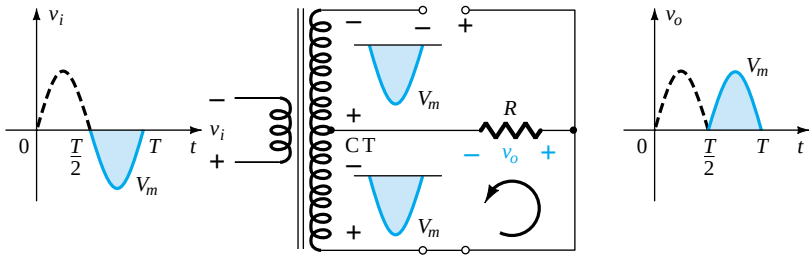

Figure 2.61 Network conditions for the negative region of v_i.

age across the load resistor R. The net effect is the same output as that appearing in Fig. 2.56 with the same dc levels.

PIV

The network of Fig. 2.62 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and V_m as established by the adjoining loop will result in

$$\text{PIV} = V_{\text{secondary}} + V_R$$
$$= V_m + V_m$$

and

$$\boxed{\text{PIV} \geqq 2V_m} \quad \text{CT transformer, full-wave rectifier} \tag{2.13}$$

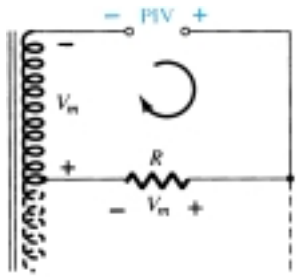

Figure 2.62 Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

EXAMPLE 2.19

Determine the output waveform for the network of Fig. 2.63 and calculate the output dc level and the required PIV of each diode.

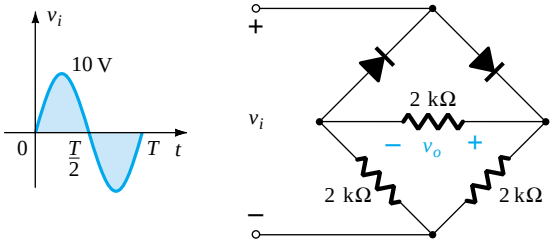

Figure 2.63 Bridge network for Example 2.19.

Solution

The network will appear as shown in Fig. 2.64 for the positive region of the input voltage. Redrawing the network will result in the configuration of Fig. 2.65, where $v_o = \frac{1}{2}v_i$ or $V_{o_{\max}} = \frac{1}{2}V_{i_{\max}} = \frac{1}{2}(10\text{ V}) = 5\text{ V}$, as shown in Fig. 2.65. For the negative part of the input the roles of the diodes will be interchanged and v_o will appear as shown in Fig. 2.66.

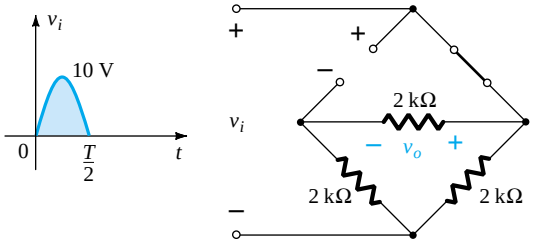

Figure 2.64 Network of Fig. 2.63 for the positive region of v_i.

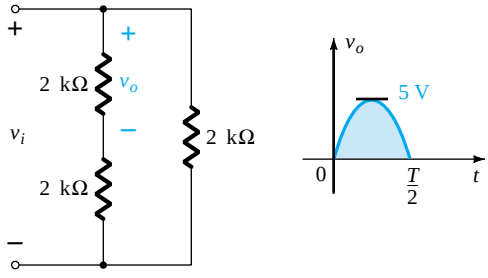

Figure 2.65 Redrawn network of Fig. 2.64.

The effect of removing two diodes from the bridge configuration was therefore to reduce the available dc level to the following:

$$V_{\text{dc}} = 0.636(5\text{ V}) = \mathbf{3.18\text{ V}}$$

or that available from a half-wave rectifier with the same input. However, the PIV as determined from Fig. 2.58 is equal to the maximum voltage across R, which is 5 V or half of that required for a half-wave rectifier with the same input.

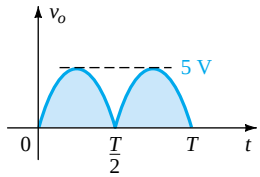

Figure 2.66 Resulting output for Example 2.19.

2.9 CLIPPERS

There are a variety of diode networks called *clippers* that have the ability to "clip" off a portion of the input signal without distorting the remaining part of the alternating waveform. The half-wave rectifier of Section 2.7 is an example of the simplest form of diode clipper—one resistor and diode. Depending on the orientation of the diode, the positive or negative region of the input signal is "clipped" off.

There are two general categories of clippers: *series* and *parallel*. The series configuration is defined as one where the diode is in series with the load, while the parallel variety has the diode in a branch parallel to the load.

Series

The response of the series configuration of Fig. 2.67a to a variety of alternating waveforms is provided in Fig. 2.67b. Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper. The addition of a dc supply such as shown in Fig. 2.68 can have a pronounced effect on the output of a clipper. Our initial discussion will be limited to ideal diodes, with the effect of V_T reserved for a concluding example.

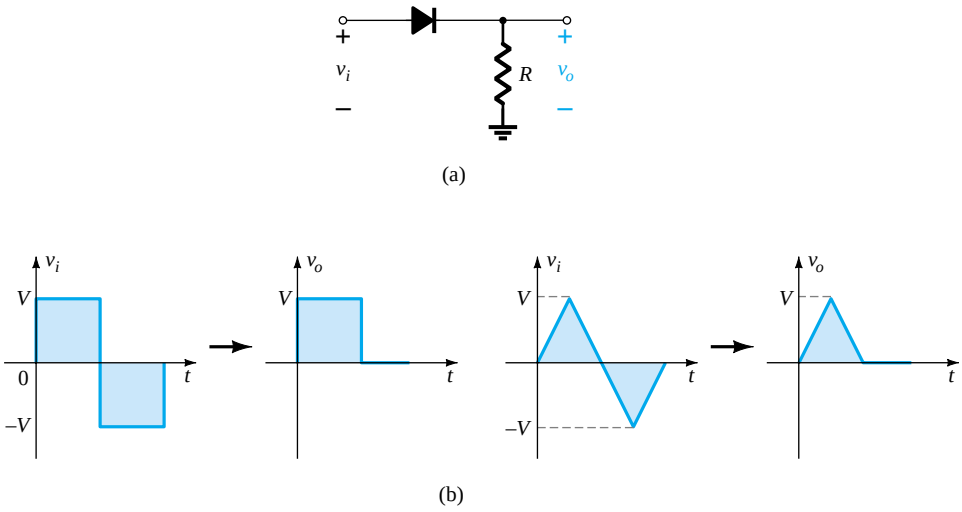

Figure 2.67 Series clipper.

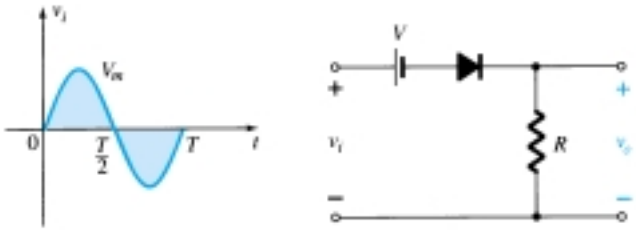

Figure 2.68 Series clipper with a dc supply.

There is no general procedure for analyzing networks such as the type in Fig. 2.68, but there are a few thoughts to keep in mind as you work toward a solution.

1. *Make a mental sketch of the response of the network based on the direction of the diode and the applied voltage levels.*

For the network of Fig. 2.68, the direction of the diode suggests that the signal v_i must be positive to turn it on. The dc supply further requires that the voltage v_i be greater than V volts to turn the diode on. The negative region of the input signal is

"pressuring" the diode into the "off" state, supported further by the dc supply. In general, therefore, we can be quite sure that the diode is an open circuit ("off" state) for the negative region of the input signal.

2. *Determine the applied voltage (transition voltage) that will cause a change in state for the diode.*

For the ideal diode the transition between states will occur at the point on the characteristics where $v_d = 0$ V and $i_d = 0$ A. Applying the condition $i_d = 0$ at $v_d = 0$ to the network of Fig. 2.68 will result in the configuration of Fig. 2.69, where it is recognized that the level of v_i that will cause a transition in state is

$$v_i = V \tag{2.14}$$

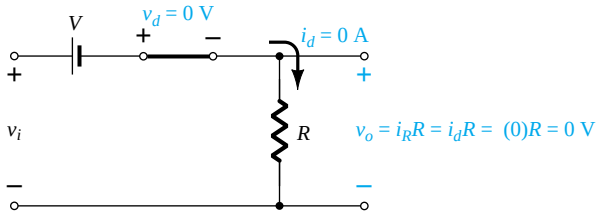

Figure 2.69 Determining the transition level for the circuit of Fig. 2.68.

For an input voltage greater than V volts the diode is in the short-circuit state, while for input voltages less than V volts it is in the open-circuit or "off" state.

3. *Be continually aware of the defined terminals and polarity of v_o.*

When the diode is in the short-circuit state, such as shown in Fig. 2.70, the output voltage v_o can be determined by applying Kirchhoff's voltage law in the clockwise direction:

$$v_i - V - v_o = 0 \text{ (CW direction)}$$

and

$$v_o = v_i - V \tag{2.15}$$

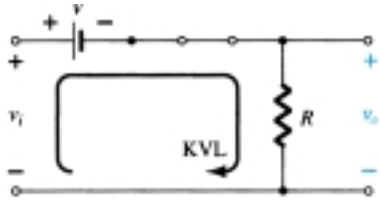

Figure 2.70 Determining v_o.

4. *It can be helpful to sketch the input signal above the output and determine the output at instantaneous values of the input.*

It is then possible that the output voltage can be sketched from the resulting data points of v_o as demonstrated in Fig. 2.71. Keep in mind that at an instantaneous value of v_i the input can be treated as a dc supply of that value and the corresponding dc value (the instantaneous value) of the output determined. For instance, at $v_i = V_m$ for the network of Fig. 2.68, the network to be analyzed appears in Fig. 2.72. For $V_m > V$ the diode is in the short-circuit state and $v_o = V_m - V$, as shown in Fig. 2.71.

At $v_i = V$ the diodes change state; at $v_i = -V_m$, $v_o = 0$ V; and the complete curve for v_o can be sketched as shown in Fig. 2.73.

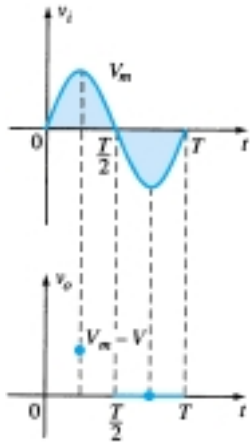

Figure 2.71 Determining levels of v_o.

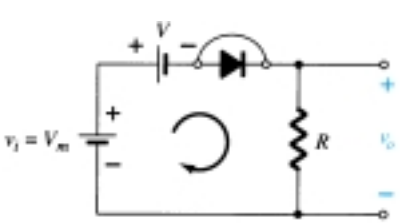

Figure 2.72 Determining v_o when $v_i = V_m$.

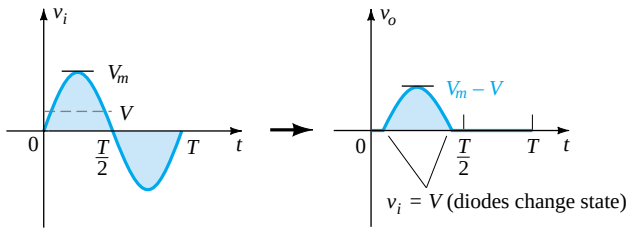

Figure 2.73 Sketching v_o.

EXAMPLE 2.20

Determine the output waveform for the network of Fig. 2.74.

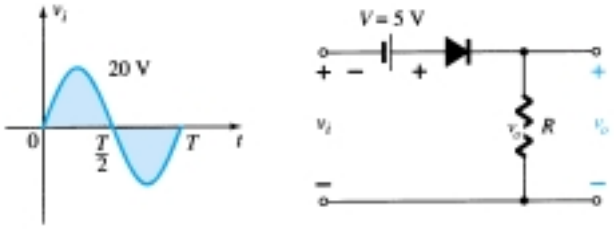

Figure 2.74 Series clipper for Example 2.20.

Solution

Past experience suggests that the diode will be in the "on" state for the positive region of v_i—especially when we note the aiding effect of $V = 5$ V. The network will then appear as shown in Fig. 2.75 and $v_o = v_i + 5$ V. Substituting $i_d = 0$ at $v_d = 0$ for the transition levels, we obtain the network of Fig. 2.76 and $v_i = -5$ V.

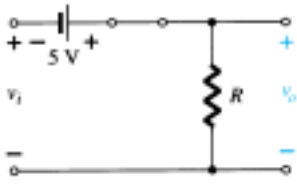

Figure 2.75 v_o with diode in the "on" state.

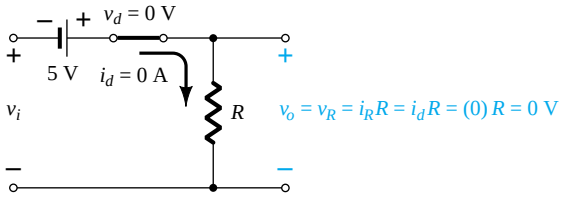

Figure 2.76 Determining the transition level for the clipper of Fig. 2.74.

For v_i more negative than -5 V the diode will enter its open-circuit state, while for voltages more positive than -5 V the diode is in the short-circuit state. The input and output voltages appear in Fig. 2.77.

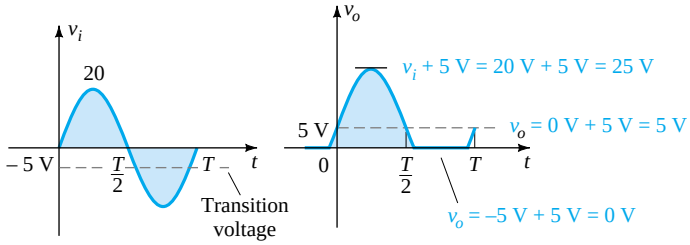

Figure 2.77 Sketching v_o for Example 2.20.

The analysis of clipper networks with square-wave inputs is actually easier to analyze than with sinusoidal inputs because only two levels have to be considered. In other words, the network can be analyzed as if it had two dc level inputs with the resulting output v_o plotted in the proper time frame.

Repeat Example 2.20 for the square-wave input of Fig. 2.78. *EXAMPLE 2.21*

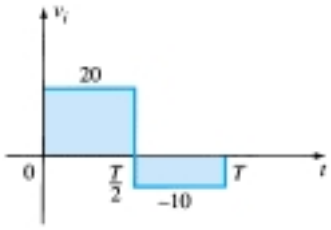

Figure 2.78 Applied signal for Example 2.21.

Solution

For $v_i = 20$ V $(0 \rightarrow T/2)$ the network of Fig. 2.79 will result. The diode is in the short-circuit state and $v_o = 20$ V + 5 V = 25 V. For $v_i = -10$ V the network of Fig. 2.80 will result, placing the diode in the "off" state and $v_o = i_R R = (0)R = 0$ V. The resulting output voltage appears in Fig. 2.81.

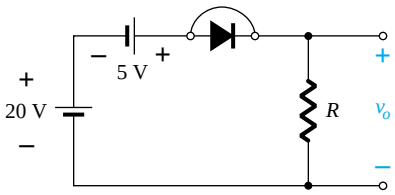

Figure 2.79 v_o at $v_i = +20$ V.

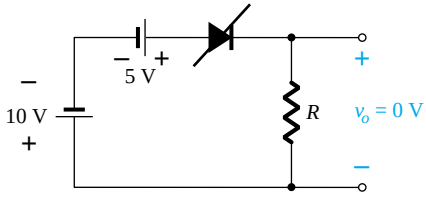

Figure 2.80 v_o at $v_i = -10$ V.

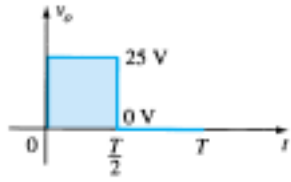

Figure 2.81 Sketching v_o for Example 2.21.

Note in Example 2.21 that the clipper not only clipped off 5 V from the total swing but raised the dc level of the signal by 5 V.

Parallel

The network of Fig. 2.82 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.67. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

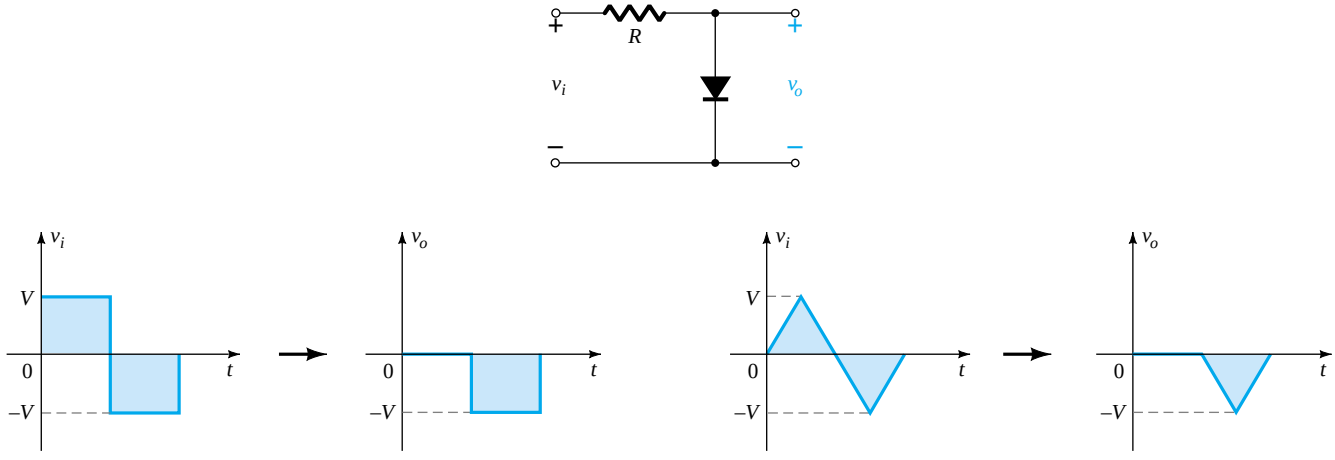

Figure 2.82 Response to a parallel clipper.

EXAMPLE 2.2

Determine v_o for the network of Fig. 2.83.

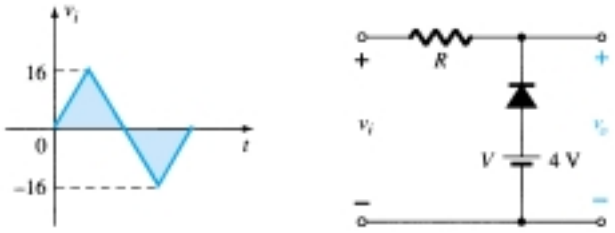

Figure 2.83 Example 2.22.

Solution

The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for the negative region of the input signal. For this region the network will appear as shown in Fig. 2.84, where the defined terminals for v_o require that $v_o = V = 4$ V.

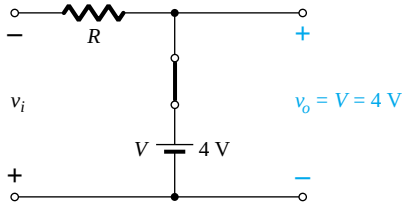

Figure 2.84 v_o for the negative region of v_i.

The transition state can be determined from Fig. 2.85, where the condition $i_d = 0$ A at $v_d = 0$ V has been imposed. The result is v_i (transition) $= V = 4$ V.

Since the dc supply is obviously "pressuring" the diode to stay in the short-circuit state, the input voltage must be greater than 4 V for the diode to be in the "off" state. Any input voltage less than 4 V will result in a short-circuited diode.

For the open-circuit state the network will appear as shown in Fig. 2.86, where $v_o = v_i$. Completing the sketch of v_o results in the waveform of Fig. 2.87.

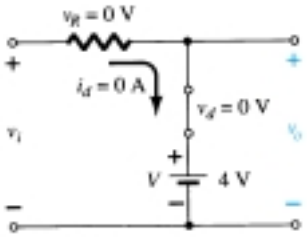

Figure 2.85 Determining the transition level for Example 2.22.

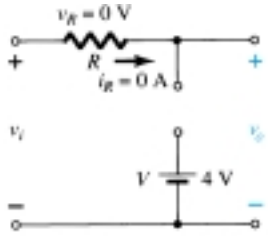

Figure 2.86 Determining v_o for the open state of the diode.

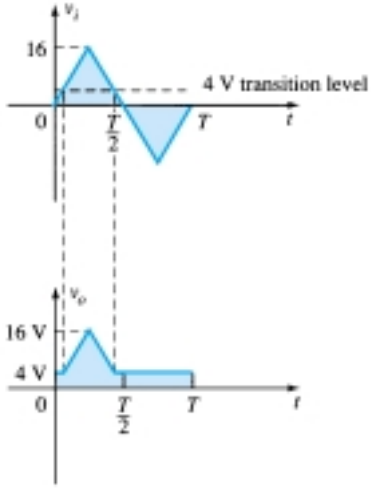

Figure 2.87 Sketching v_o for Example 2.22.

To examine the effects of V_T on the output voltage, the next example will specify a silicon diode rather than an ideal diode equivalent.

Repeat Example 2.22 using a silicon diode with $V_T = 0.7$ V. *EXAMPLE 2.23*

Solution

The transition voltage can first be determined by applying the condition $i_d = 0$ A at $v_d = V_D = 0.7$ V and obtaining the network of Fig. 2.88. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_T - V = 0$$

and

$$v_i = V - V_T = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3\ V}$$

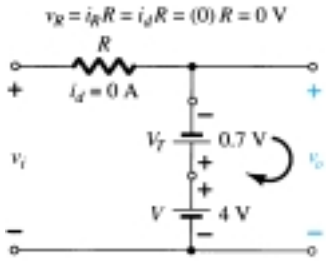

Figure 2.88 Determining the transition level for the network of Fig. 2.83.

For input voltages greater than 3.3 V, the diode will be an open circuit and $v_o = v_i$. For input voltages of less than 3.3 V, the diode will be in the "on" state and the network of Fig. 2.89 results, where

$$v_o = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3\ V}$$

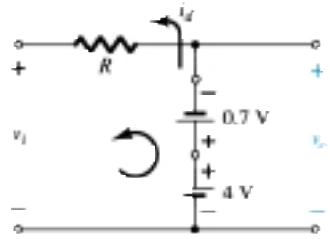

Figure 2.89 Determining v_o for the diode of Fig. 2.83 in the "on" state.

The resulting output waveform appears in Fig. 2.90. Note that the only effect of V_T was to drop the transition level to 3.3 from 4 V.

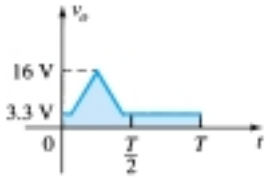

Figure 2.90 Sketching v_o for Example 2.23.

There is no question that including the effects of V_T will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of V_T, will not be that difficult.

Summary

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 2.91. In particular, note the response of the last configuration, with its ability to clip off a positive and a negative section as determined by the magnitude of the dc supplies.

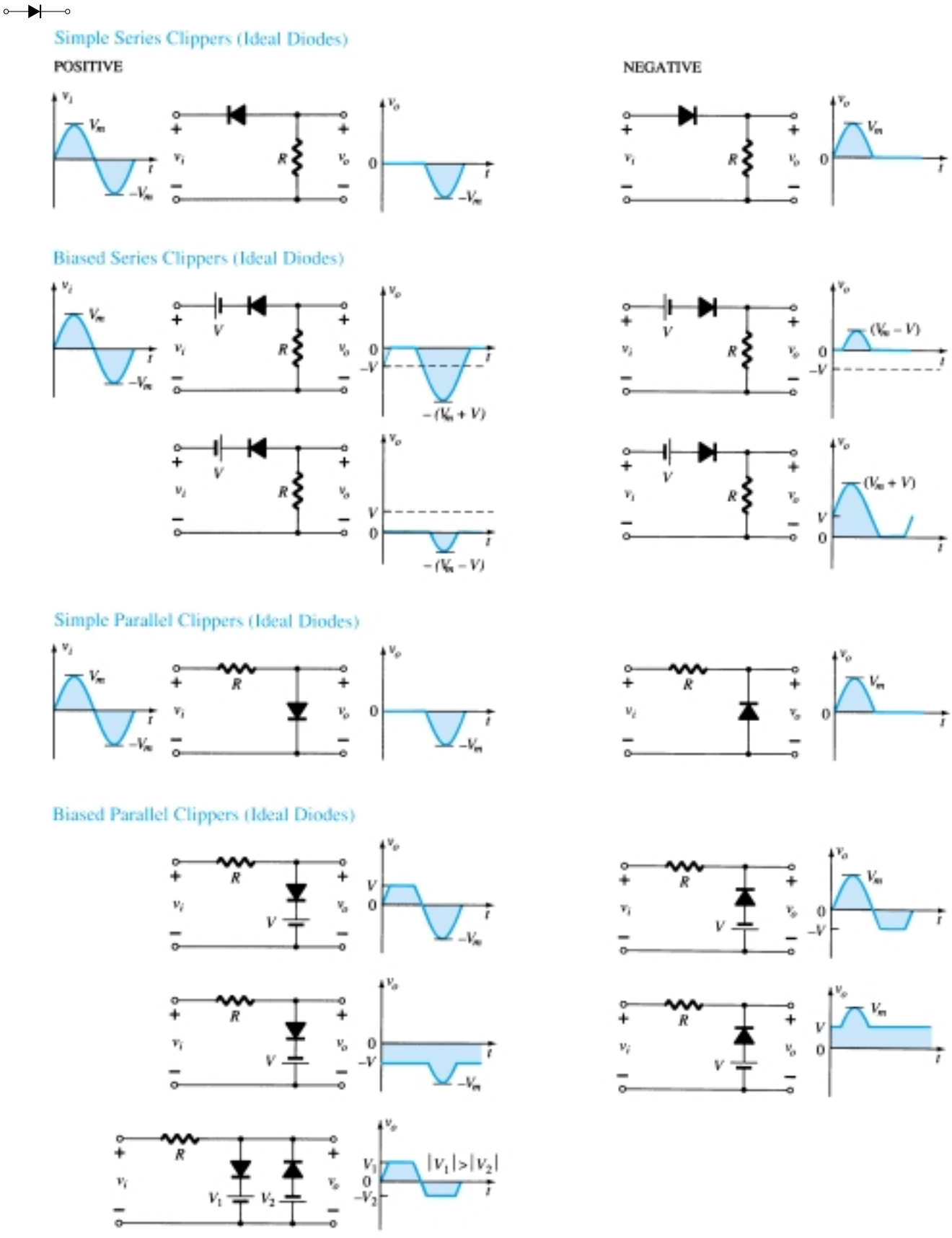

Figure 2.91 Clipping circuits.

2.10 CLAMPERS

The *clamping* network is one that will "clamp" a signal to a different dc level. The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants.

The network of Fig. 2.92 will clamp the input signal to the zero level (for ideal diodes). The resistor R can be the load resistor or a parallel combination of the load resistor and a resistor designed to provide the desired level of R.

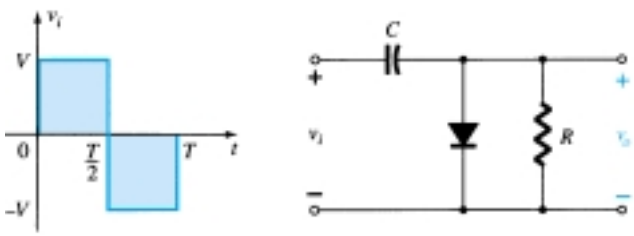

Figure 2.92 Clamper.

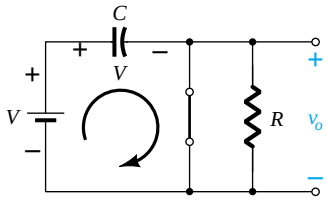

Figure 2.93 Diode "on" and the capacitor charging to V volts.

During the interval $0 \rightarrow T/2$ the network will appear as shown in Fig. 2.93, with the diode in the "on" state effectively "shorting out" the effect of the resistor R. The resulting RC time constant is so small (R determined by the inherent resistance of the network) that the capacitor will charge to V volts very quickly. During this interval the output voltage is directly across the short circuit and $v_o = 0$ V.

When the input switches to the $-V$ state, the network will appear as shown in Fig. 2.94, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5τ much greater than the period $T/2 \rightarrow T$, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

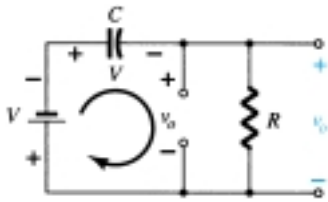

Figure 2.94 Determining v_o with the diode "off."

Since v_o is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.94. Applying Kirchhoff's voltage law around the input loop will result in

$$-V - V - v_o = 0$$

and

$$v_o = -2V$$

The negative sign resulting from the fact that the polarity of $2V$ is opposite to the polarity defined for v_o. The resulting output waveform appears in Fig. 2.95 with the input signal. The output signal is clamped to 0 V for the interval 0 to $T/2$ but maintains the same total swing ($2V$) as the input.

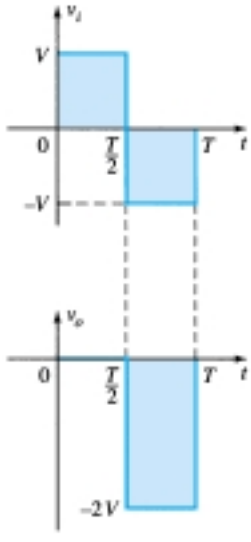

Figure 2.95 Sketching v_o for the network of Fig. 2.92.

For a clamping network:

The total swing of the output is equal to the total swing of the input signal.

This fact is an excellent checking tool for the result obtained.

In general, the following steps may be helpful when analyzing clamping networks:

1. *Start the analysis of clamping networks by considering that part of the input signal that will forward bias the diode.*

The statement above may require skipping an interval of the input signal (as demonstrated in an example to follow), but the analysis will not be extended by an unnecessary measure of investigation.

2. *During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the network.*
3. *Assume that during the period when the diode is in the "off" state the capacitor will hold on to its established voltage level.*
4. *Throughout the analysis maintain a continual awareness of the location and reference polarity for v_o to ensure that the proper levels for v_o are obtained.*
5. *Keep in mind the general rule that the total swing of the total output must match the swing of the input signal.*

EXAMPLE 2.24

Determine v_o for the network of Fig. 2.96 for the input indicated.

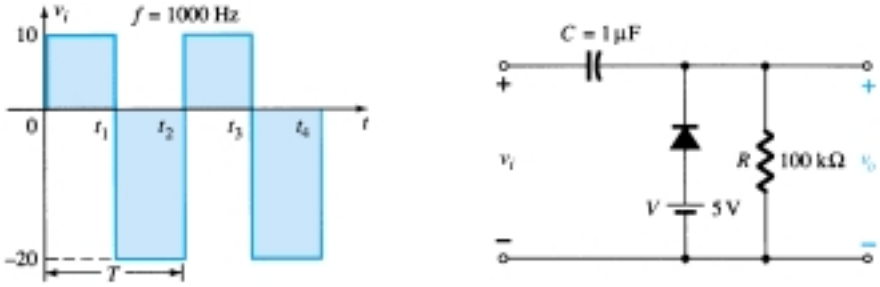

Figure 2.96 Applied signal and network for Example 2.24.

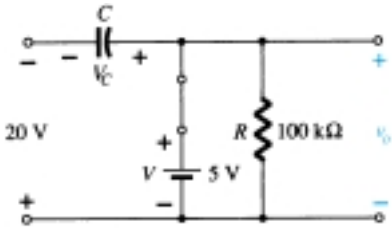

Figure 2.97 Determining v_o and V_C with the diode in the "on" state.

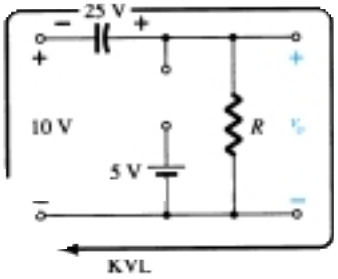

Figure 2.98 Determining v_o with the diode in the "off" state.

Solution

Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state as recommended by comment 1. For this interval the network will appear as shown in Fig. 2.97. The output is across R, but it is also directly across the 5-V battery if you follow the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5$ V for this interval. Applying Kirchhoff's voltage law around the input loop will result in

$$-20\text{ V} + V_C - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V}$$

The capacitor will therefore charge up to 25 V, as stated in comment 2. In this case the resistor R is not shorted out by the diode but a Thévenin equivalent circuit of that portion of the network which includes the battery and the resistor will result in $R_{Th} = 0\ \Omega$ with $E_{Th} = V = 5$ V. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.98.

The open-circuit equivalent for the diode will remove the 5-V battery from having any effect on v_o, and applying Kirchhoff's voltage law around the outside loop of the network will result in

$$+10\text{ V} + 25\text{ V} - v_o = 0$$

and

$$v_o = 35\text{ V}$$

The time constant of the discharging network of Fig. 2.98 is determined by the product RC and has the magnitude

$$\tau = RC = (100\ \text{k}\Omega)(0.1\ \mu\text{F}) = 0.01\ \text{s} = 10\ \text{ms}$$

The total discharge time is therefore $5\tau = 5(10\ \text{ms}) = 50\ \text{ms}$.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.99 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

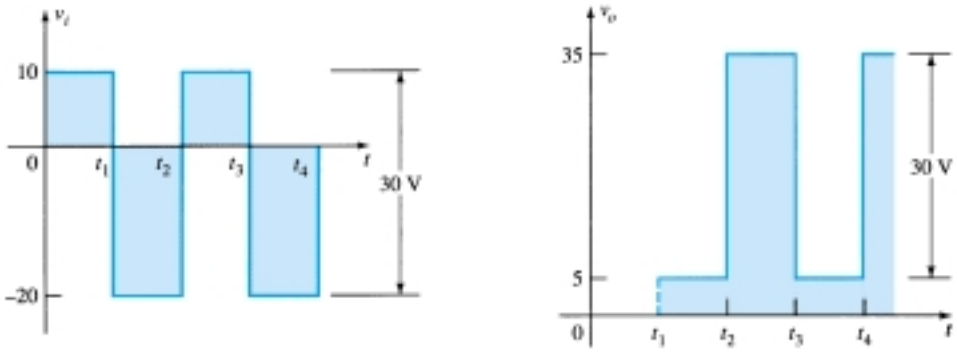

Figure 2.99 v_i and v_o for the clamper of Fig. 2.96.

EXAMPLE 2.25

Repeat Example 2.24 using a silicon diode with $V_T = 0.7$ V.

Solution

For the short-circuit state the network now takes on the appearance of Fig. 2.100 and v_o can be determined by Kirchhoff's voltage law in the output section.

$$+5\ \text{V} - 0.7\ \text{V} - v_o = 0$$

and

$$v_o = 5\ \text{V} - 0.7\ \text{V} = 4.3\ \text{V}$$

For the input section Kirchhoff's voltage law will result in

$$-20\ \text{V} + V_C + 0.7\ \text{V} - 5\ \text{V} = 0$$

and

$$V_C = 25\ \text{V} - 0.7\ \text{V} = 24.3\ \text{V}$$

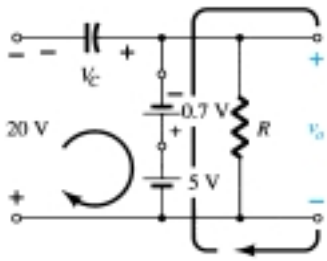

Figure 2.100 Determining v_o and V_C with the diode in the "on" state.

For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.101, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10\ \text{V} + 24.3\ \text{V} - v_o = 0$$

and

$$v_o = 34.3\ \text{V}$$

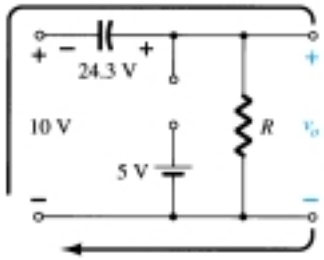

Figure 2.101 Determining v_o with the diode in the open state.

The resulting output appears in Fig. 2.102, verifying the statement that the input and output swings are the same.

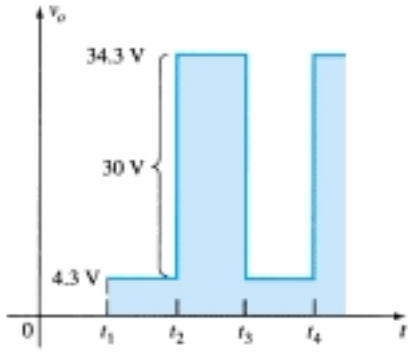

Figure 2.102 Sketching v_o for the clamper of Fig. 2.96 with a silicon diode.

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.103. Although all the waveforms appearing in Fig. 2.103 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.104 for a network appearing in the bottom right of Fig. 2.103.

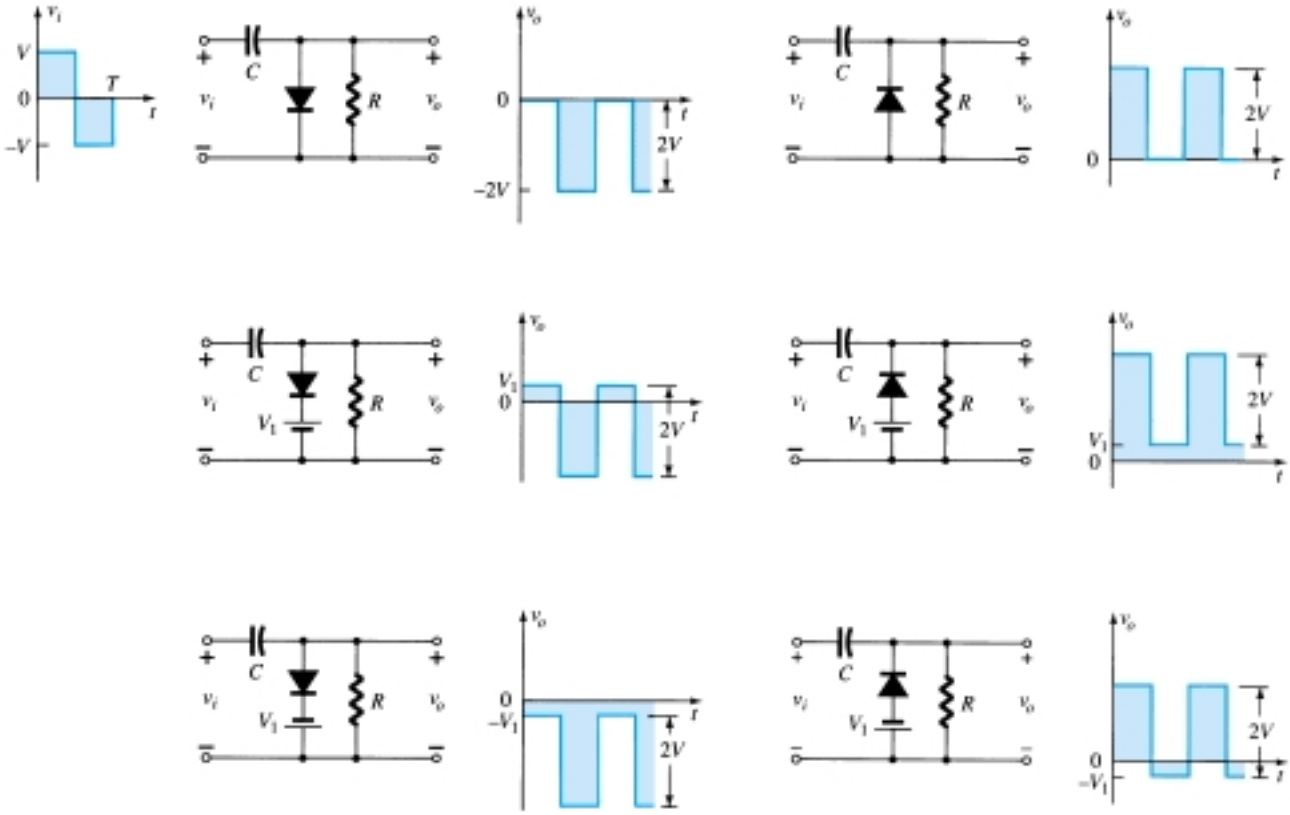

Figure 2.103 Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

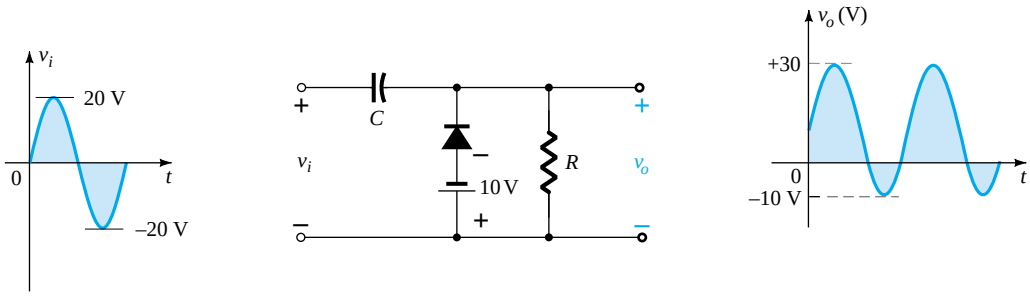

Figure 2.104 Clamping network with a sinusoidal input.

2.11 ZENER DIODES

The analysis of networks employing Zener diodes is quite similar to that applied to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Unless otherwise specified, the Zener model to be employed for the "on" state will be as shown in Fig. 2.105a. For the "off" state as defined by a voltage less than V_Z but greater than 0 V with the polarity indicated in Fig. 2.105b, the Zener equivalent is the open circuit that appears in the same figure.

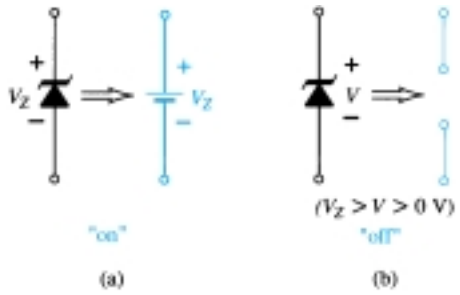

Figure 2.105 Zener diode equivalents for the (a) "on" and (b) "off" states.

V_i and R

The simplest of Zener diode networks appears in Fig. 2.106. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

1. *Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.*

Applying step 1 to the network of Fig. 2.106 will result in the network of Fig. 2.107, where an application of the voltage divider rule will result in

$$V = V_L = \frac{R_L V_i}{R + R_L} \tag{2.16}$$

If $V \geq V_Z$, the Zener diode is "on" and the equivalent model of Fig. 2.105a can be substituted. If $V < V_Z$, the diode is "off" and the open-circuit equivalence of Fig. 2.105b is substituted.

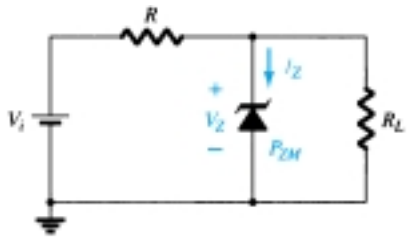

Figure 2.106 Basic Zener regulator.

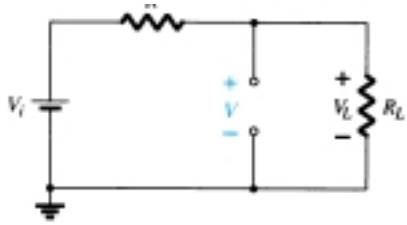

Figure 2.107 Determining the state of the Zener diode.

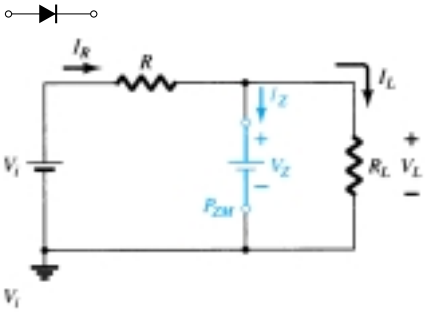

Figure 2.108 Substituting the Zener equivalent for the "on" situation.

2. Substitute the appropriate equivalent circuit and solve for the desired unknowns.

For the network of Fig. 2.106, the "on" state will result in the equivalent network of Fig. 2.108. Since voltages across parallel elements must be the same, we find that

$$V_L = V_Z \tag{2.17}$$

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

and

$$I_Z = I_R - I_L \tag{2.18}$$

where

$$I_L = \frac{V_L}{R_L} \quad \textit{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z \tag{2.19}$$

which must be less than the P_{ZM} specified for the device.

Before continuing, it is particularly important to realize that the first step was employed only to determine the *state of the Zener diode*. If the Zener diode is in the "on" state, the voltage across the diode is not V volts. When the system is turned on, the Zener diode will turn "on" as soon as the voltage across the Zener diode is V_Z volts. It will then "lock in" at this level and never reach the higher level of V volts.

Zener diodes are most frequently used in *regulator* networks or as a *reference* voltage. Figure 2.106 is a simple regulator designed to maintain a fixed voltage across the load R_L. For values of applied voltage greater than required to turn the Zener diode "on," the voltage across the load will be maintained at V_Z volts. If the Zener diode is employed as a reference voltage, it will provide a level for comparison against other voltages.

EXAMPLE 2.26

(a) For the Zener diode network of Fig. 2.109, determine V_L, V_R, I_Z, and P_Z.
(b) Repeat part (a) with $R_L = 3\ \text{k}\Omega$.

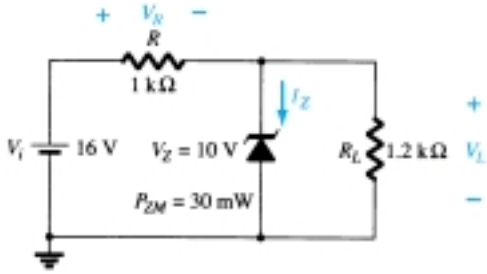

Figure 2.109 Zener diode regulator for Example 2.26.

Solution

(a) Following the suggested procedure the network is redrawn as shown in Fig. 2.110. Applying Eq. (2.16) gives

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 1.2\ \text{k}\Omega} = 8.73\ \text{V}$$

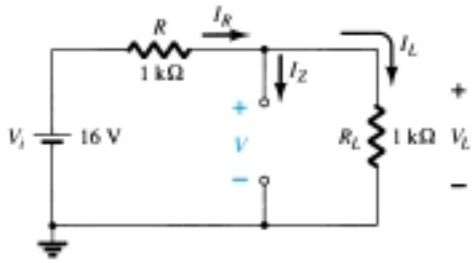

Figure 2.110 Determining V for the regulator of Fig. 2.109.

Since $V = 8.73$ V is less than $V_Z = 10$ V, the diode is in the "off" state as shown on the characteristics of Fig. 2.111. Substituting the open-circuit equivalent will result in the same network as in Fig. 2.110, where we find that

$$V_L = V = \mathbf{8.73\ V}$$

$$V_R = V_i - V_L = 16\ V - 8.73\ \text{V} = \mathbf{7.27\ V}$$

$$I_Z = \mathbf{0\ A}$$

and

$$P_Z = V_Z I_Z = V_Z(0\ \text{A}) = \mathbf{0\ W}$$

(b) Applying Eq. (2.16) will now result in

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 3\ \text{k}\Omega} = 12\ \text{V}$$

Since $V = 12$ V is greater than $V_Z = 10$ V, the diode is in the "on" state and the network of Fig. 2.112 will result. Applying Eq. (2.17) yields

$$V_L = V_Z = \mathbf{10\ V}$$

and

$$V_R = V_i - V_L = 16\ \text{V} - 10\ \text{V} = \mathbf{6\ V}$$

with

$$I_L = \frac{V_L}{R_L} = \frac{10\ \text{V}}{3\ \text{k}\Omega} = 3.33\ \text{mA}$$

and

$$\text{I}_R = \frac{V_R}{R} = \frac{6\ \text{V}}{1\ \text{k}\Omega} = 6\ \text{mA}$$

so that

$$I_Z = I_R - I_L\ \text{[Eq. (2.18)]}$$

$$= 6\ \text{mA} - 3.33\ \text{mA}$$

$$= \mathbf{2.67\ mA}$$

The power dissipated,

$$P_Z = V_Z I_Z = (10\ \text{V})(2.67\ \text{mA}) = \mathbf{26.7\ mW}$$

which is less than the specified $P_{ZM} = 30$ mW.

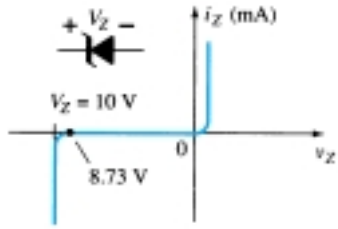

Figure 2.111 Resulting operating point for the network of Fig. 2.109.

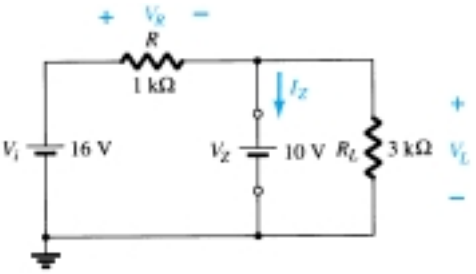

Figure 2.112 Network of Fig. 2.109 in the "on" state.

Fixed V_i, Variable R_L

Due to the offset voltage V_Z, there is a specific range of resistor values (and therefore load current) which will ensure that the Zener is in the "on" state. Too small a load resistance R_L will result in a voltage V_L across the load resistor less than V_Z, and the Zener device will be in the "off" state.

To determine the minimum load resistance of Fig. 2.106 that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for R_L, we have

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} \tag{2.20}$$

Any load resistance value greater than the R_L obtained from Eq. (2.20) will ensure that the Zener diode is in the "on" state and the diode can be replaced by its V_Z source equivalent.

The condition defined by Eq. (2.20) establishes the minimum R_L but in turn specifies the maximum I_L as

$$I_{L_{\max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\min}}} \tag{2.21}$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$V_R = V_i - V_Z \tag{2.22}$$

and I_R remains fixed at

$$I_R = \frac{V_R}{R} \tag{2.23}$$

The Zener current

$$I_Z = I_R - I_L \tag{2.24}$$

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value since I_R is constant.

Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$I_{L_{\min}} = I_R - I_{ZM} \tag{2.25}$$

and the maximum load resistance as

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} \tag{2.26}$$

EXAMPLE 2.27

(a) For the network of Fig. 2.113, determine the range of R_L and I_L that will result in V_{R_L} being maintained at 10 V.
(b) Determine the maximum wattage rating of the diode.

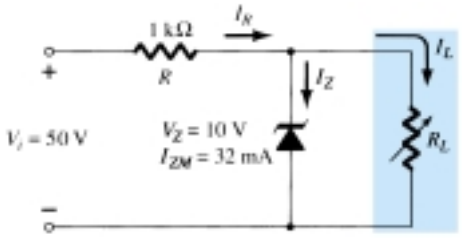

Figure 2.113 Voltage regulator for Example 2.27.

Solution

(a) To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1\text{ k}\Omega)(10\text{ V})}{50\text{ V} - 10\text{ V}} = \frac{10\text{ k}\Omega}{40} = \mathbf{250\ \Omega}$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50\text{ V} - 10\text{ V} = \mathbf{40\ V}$$

and Eq. (2.23) provides the magnitude of I_R:

$$I_R = \frac{V_R}{R} = \frac{40\text{ V}}{1\text{ k}\Omega} = \mathbf{40\ mA}$$

The minimum level of I_L is then determined by Eq. (2.25):

$$I_{L_{\min}} = I_R - I_{ZM} = 40\text{ mA} - 32\text{ mA} = \mathbf{8\ mA}$$

with Eq. (2.26) determining the maximum value of R_L:

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} = \frac{10\text{ V}}{8\text{ mA}} = \mathbf{1.25\ k\Omega}$$

A plot of V_L versus R_L appears in Fig. 2.114a and for V_L versus I_L in Fig. 2.114b.

(b) $P_{\max} = V_Z\, I_{ZM}$
$= (10\text{ V})(32\text{ mA}) = \mathbf{320\ mW}$

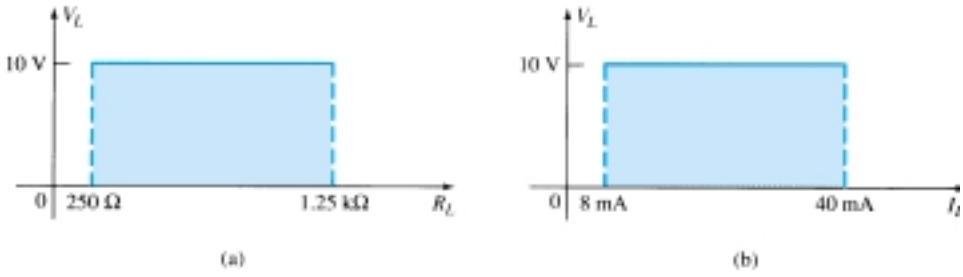

Figure 2.114 V_L versus R_L and I_L for the regulator of Fig. 2.113.

Fixed R_L, Variable V_i

For fixed values of R_L in Fig. 2.106, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = V_{i_{min}}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

and

$$\boxed{V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L}} \tag{2.27}$$

The maximum value of V_i is limited by the maximum Zener current I_{ZM}. Since $I_{ZM} = I_R - I_L$,

$$\boxed{I_{R_{max}} = I_{ZM} + I_L} \tag{2.28}$$

Since I_L is fixed at V_Z/R_L and I_{ZM} is the maximum value of I_Z, the maximum V_i is defined by

$$V_{i_{max}} = V_{R_{max}} + V_Z$$

$$\boxed{V_{i_{max}} = I_{R_{max}}R + V_Z} \tag{2.29}$$

EXAMPLE 2.28

Determine the range of values of V_i that will maintain the Zener diode of Fig. 2.115 in the "on" state.

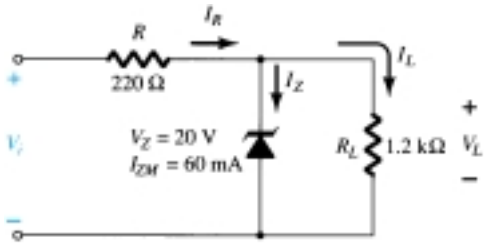

Figure 2.115 Regulator for Example 2.28.

Solution

$$\text{Eq. (2.27):}\quad V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200\ \Omega + 220\ \Omega)(20\ \text{V})}{1200\ \Omega} = \mathbf{23.67\ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20\ \text{V}}{1.2\ \text{k}\Omega} = 16.67\ \text{mA}$$

$$\text{Eq. (2.28):}\quad I_{R_{max}} = I_{ZM} + I_L = 60\ \text{mA} + 16.67\ \text{mA}$$
$$= 76.67\ \text{mA}$$

$$\text{Eq. (2.29):}\quad V_{i_{max}} = I_{R_{max}}R + V_Z$$
$$= (76.67\ \text{mA})(0.22\ \text{k}\Omega) + 20\ \text{V}$$
$$= 16.87\ \text{V} + 20\ \text{V}$$
$$= \mathbf{36.87\ V}$$

A plot of V_L versus V_i is provided in Fig. 2.116.

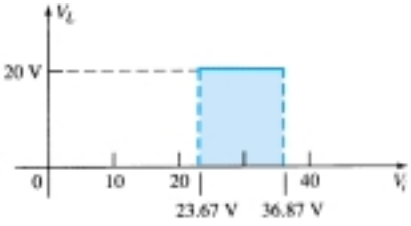

Figure 2.116 V_L versus V_i for the regulator of Fig. 2.115.

The results of Example 2.28 reveal that for the network of Fig. 2.115 with a fixed R_L, the output voltage will remain fixed at 20 V for a range of input voltage that extends from 23.67 to 36.87 V.

In fact, the input could appear as shown in Fig. 2.117 and the output would remain constant at 20 V, as shown in Fig. 2.116. The waveform appearing in Fig. 2.117 is obtained by *filtering* a half-wave- or full-wave-rectified output—a process described in detail in a later chapter. The net effect, however, is to establish a steady dc voltage (for a defined range of V_i) such as that shown in Fig. 2.116 from a sinusoidal source with 0 average value.

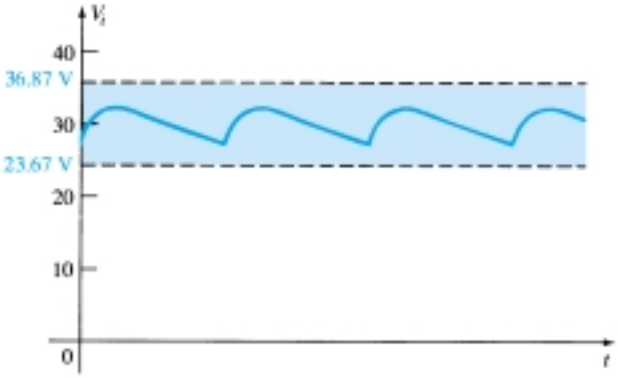

Figure 2.117 Waveform generated by a filtered rectified signal.

Two or more reference levels can be established by placing Zener diodes in series as shown in Fig. 2.118. As long as V_i is greater than the sum of V_{Z_1} and V_{Z_2}, both diodes will be in the "on" state and the three reference voltages will be available.

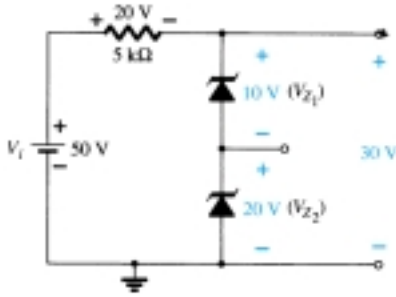

Figure 2.118 Establishing three reference voltage levels.

Two back-to-back Zeners can also be used as an ac regulator as shown in Fig. 2.119a. For the sinusoidal signal v_i the circuit will appear as shown in Fig. 2.119b at the instant $v_i = 10$ V. The region of operation for each diode is indicated in the adjoining figure. Note that Z_1 is in a low-impedance region, while the impedance of Z_2 is quite large, corresponding with the open-circuit representation. The result is that $v_o = v_i$ when $v_i = 10$ V. The input and output will continue to duplicate each other until v_i reaches 20 V. Z_2 will then "turn on" (as a Zener diode), while Z_1 will be in a

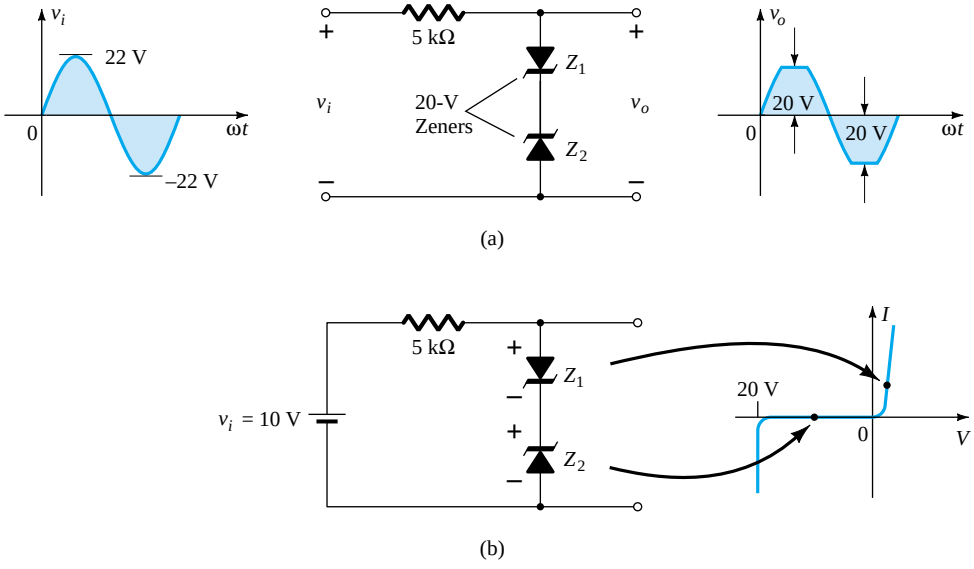

Figure 2.119 Sinusoidal ac regulation: (a) 40-V peak-to-peak sinusoidal ac regulator; (b) circuit operation at $v_i = 10$ V.

region of conduction with a resistance level sufficiently small compared to the series 5-kΩ resistor to be considered a short circuit. The resulting output for the full range of v_i is provided in Fig. 2.119(a). Note that the waveform is not purely sinusoidal, but its rms value is lower than that associated with a full 22-V peak signal. The network is effectively limiting the rms value of the available voltage. The network of Fig. 2.119a can be extended to that of a simple square-wave generator (due to the clipping action) if the signal v_i is increased to perhaps a 50-V peak with 10-V Zeners as shown in Fig. 2.120 with the resulting output waveform.

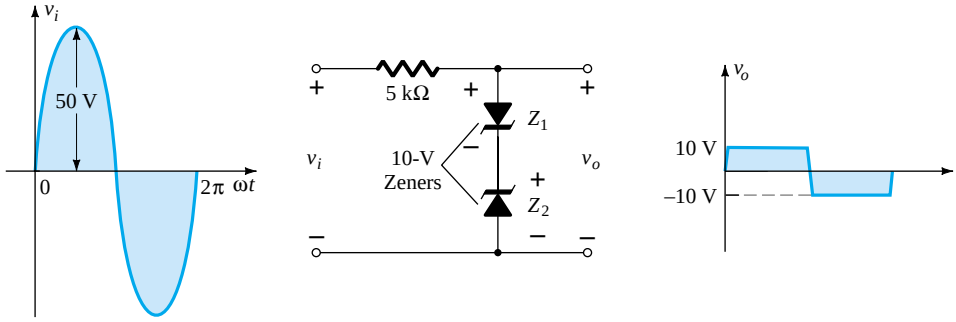

Figure 2.120 Simple square-wave generator.

2.12 VOLTAGE-MULTIPLIER CIRCUITS

Voltage-multiplier circuits are employed to maintain a relatively low transformer peak voltage while stepping up the peak output voltage to two, three, four, or more times the peak rectified voltage.

Voltage Doubler

The network of Figure 2.121 is a half-wave voltage doubler. During the positive voltage half-cycle across the transformer, secondary diode D_1 conducts (and diode D_2 is cut off), charging capacitor C_1 up to the peak rectified voltage (V_m). Diode D_1 is ideally a short during this half-cycle, and the input voltage charges capacitor C_1 to V_m with the polarity shown in Fig. 2.122a. During the negative half-cycle of the secondary voltage, diode D_1 is cut off and diode D_2 conducts charging capacitor C_2. Since diode D_2 acts as a short during the negative half-cycle (and diode D_1 is open), we can sum the voltages around the outside loop (see Fig. 2.122b):

$$-V_m - V_{C_1} + V_{C_2} = 0$$

$$-V_m - V_m + V_{C_2} = 0$$

from which

$$V_{C_2} = 2V_m$$

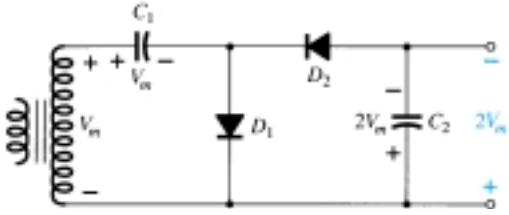

Figure 2.121 Half-wave voltage doubler.