كلية المأمون الجامعة
قسم هندسة تقنيات الحاسوب
المرحلة الثانية

أساسيات الالكترونيك التناظري

Analog Electronic Fundamentals

الجزء الأول

Chapter : 1 + 2

الدكتور
حسن وريوش حلو

الفصل الأول من العام الدراسي : ٢٠٢٤ ـ ٢٠٢٥

مفردات مادة الالكترونيك - مسار بولونيا ***Contents***

رمز المادة	إسم المادة	
BCTE 202-S1	Analog Electronic Fundamentals	أساسيات الالكترونيك التناظري

ECTS	C	P	T	أهداف المادة: التعرف على اهم الدوائر الالكترونية الأساسية المستخدمة في الأجهزة والمعدات الالكترونية.
5	3	2	2	

Week	Date	Subject		Lab	Other Activities
1	16/9 /2024	1.Introduction to electronics	Physics of material, atoms, electrons and energy bands, types of material (insulators, conductors, and semiconductors), N-type and P-type semiconductor.	Lab 1: Introduction to the Electronic Laboratory	
2	23/9		Diodes, forward bias, reverse bias, V-I characteristics.	Lab 2: Diode characteristics	
3	30/9	2.Application of diodes	Half-wave rectifier, average value, r.m.s. value, capacitor filter, ripple voltage.	Lab 3: Half-wave rectifiers	
4	7/10		Full-wave rectifier, average value, r.m.s. value, capacitor filter, ripple voltage.	Lab 4: Full-wave rectifiers	
5	14/10		Diode limiters, output voltage signal.	Lab 5: Filter for Half-wave rectifiers	
6	21/10		Clampers and Voltage Doubler.	Lab 6: Filter for Full-wave rectifiers	
7	28/10	3.Other types of diodes	Zener diodes, V-I characteristics	Lab 7: Clipping Circuits	
8	4/11		Voltage regulators using Zener diode (variable input voltage, and variable load).	Lab 8: Clamper and Voltage Doubler	
9	11/11		Zener limiters	Lab 9: Zener diode characteristics	
10	18/11		Special purpose diodes, Varactor, Light Emitting diode LED, Photo diode, Schottky diode, Tunneldiodes.	Lab 10: Voltage regulators using Zener diode	
11	25/11	4.Transistors	Bipolar junction transistor BJT, current, voltages, and parameters, maximum ratings.	Lab 11: Transistor Characteristics	
12	2/12		BJT biasing, cutoff, saturation, operating point.	Lab 12: Transistor Biasing (part 1)	
13	9/12		Transistor bias circuits, base-bias, voltage divider	Lab 13: Transistor Biasing (part 2)	
14	16/12		Transistor bias circuits, emitter-bias, collector-feedback..	Lab 14: Review	
15	-		***Final Exam.***		

Contents محتويات الملزمة

No.	subject
Chapter – 1	**Introduction to electronics:** 1-1. Physics of material, atoms, electrons and energy bands, types of material (insulators, conductors, andsemiconductors), N-type and P-type semiconductor. 1-2. Diodes, forward bias, reverse bias, V-I characteristics.
Chapter -2	**Application of diodes:** 2-1. Half-wave rectifier, average value, r.m.s. value, capacitor filter, ripple voltage. 2-2. Full-wave rectifier, average value, r.m.s. value, capacitor filter, ripple voltage. 2-3. Diode limiters, output voltage signal. 2-4. Clampers and Voltage Doubler.
Chapter – 3	**Other types of diodes:** 3-1. Zener diodes, V-I characteristics 3-2. Voltage regulators using Zener diode (variable input voltage, and variable load). 3-3. Zener limiters
Chapter – 4	**Transistors:** 4-1. Bipolar junction transistor BJT, current, voltages, and parameters, maximum ratings. 4-2. BJT biasing, cutoff, saturation, operating point. 4-3. Transistor bias circuits, base-bias, voltage divider 4-4. Transistor bias circuits, emitter-bias, collector-feedback..

References المصادر	
1.	R. Boylestad, "Electronic Devices and Circuit Theory",11th Edition
2.	بعض المصادر والمقالات من الانترنيت

كلية المأمون الجامعة

قسم هندسة تقنيات الحاسوب – لجنة النشاط العلمي

العام الدراسي ٢٠٢٤/٢٠٢٥

التقويم الجامعي ٢٠٢٤/٢٠٢٥	للمراحل ٢/٣/٤	للمرحلة الاولى
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الاثنين	٢	٩	١٦	٢٣	٣٠
الثلاثاء	٣	١٠	١٧	٢٤	
الاربعاء	٤	١١	١٨	٢٥	
الخميس	٥	١٢	١٩	٢٦	
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الأحد			٦	١٣	٢٠	٢٧
الاثنين			٧	١٤	٢١	٢٨
الثلاثاء	١	٢٨	٨	١٥	٢٢	٢٩
الاربعاء	٢	٢٩	٩	١٦	٢٣	٣٠
الخميس	٣	٣٠	١٠	١٧	٢٤	٣١
الجمعة	٤	١	١١	١٨	٢٥	

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الاثنين	٣٠	٤	١١	١٨	٢٥	
الثلاثاء	١	٥	١٢	١٩	٢٦	
الاربعاء	٢	٦	١٣	٢٠	٢٧	
الخميس	٣	٧	١٤	٢١	٢٨	
الجمعة	٤	٨	١٥	٢٢	٢٩	

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الاثنين	١	٢	٩	١٦	٣٠	
الثلاثاء	٢	٣	١٠	١٧	٣١	
الاربعاء	٣	٤	١١	١٨		
الخميس	٤	٥	١٢	١٩		
الجمعة	٥	٦	١٣	٢٠		

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الأسبوع		امتحان	عطلة ربيعية			
السبت			٤	١١	١٨	٢٥
الأحد			٥	١٢	١٩	٢٦
الاثنين			٦	١٣	٢٠	٢٧
الثلاثاء			٧	١٤	٢١	٢٨
الاربعاء	١	١	٨	١٥	٢٢	٢٩
الخميس	٢	٢	٩	١٦	٢٣	٣٠
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الأحد	٢	٣	١٠	١٧	٢٤	
الاثنين	٣	٤	١١	١٨	٢٥	
الثلاثاء	٤	٥	١٢	١٩	٢٦	
الاربعاء	٥	٦	١٣	٢٠	٢٧	
الخميس	٦	٧	١٤	٢١	٢٨	
الجمعة	٧	٨	١٥	٢٢	٢٩	

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السبت	١	٨	١٥	٢٢	٢٩	
الأحد	٢	٩	١٦	٢٣	٣٠	
الاثنين	٣	١٠	١٧	٢٤	٣١	
الثلاثاء	٤	١١	١٨	٢٥		
الاربعاء	٥	١٢	١٩	٢٦		
الخميس	٦	١٣	٢٠	٢٧		
الجمعة	٧	١٤	٢١	٢٨		

نيسان 4		شوال١٠ـ ذو القعدة١١				
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السبت			٥	١٢	١٩	٢٦
الأحد			٦	١٣	٢٠	٢٧
الاثنين			٧	١٤	٢١	٢٨
الثلاثاء	١	٣	٨	١٥	٢٢	٢٩
الاربعاء	٢	٤	٩	١٦	٢٣	٣٠
الخميس	٣	٥	١٠	١٧	٢٤	٣١
الجمعة	٤	٦	١١	١٨	٢٥	

أيار 5		ذو القعدة ١١ـ ذو الحجة١٢				
الأسبوع		امتحانات				
السبت	٣١	٤	٥	١٠	١٧	٢٤
الأحد		٥	٦	١١	١٨	٢٥
الاثنين		٦	٧	١٢	١٩	٢٦
الثلاثاء		٧	٨	١٣	٢٠	٢٧
الاربعاء		٨	٩	١٤	٢١	٢٨
الخميس	١	٩	١٠	١٥	٢٢	٢٩
الجمعة	٢	١٠	١١	١٦	٢٣	٣٠

حزيران 6		ذو الحجة١٢ـ محرم١/١٤٤٧هـ				
الأسبوع		امتحان الدور الثاني				
السبت		٧	١٤	٢١	٢٨	
الأحد	١	٨	١٥	٢٢	٢٩	
الاثنين	٢	٩	١٦	٢٣	٣٠	
الثلاثاء	٣	١٠	١٧	٢٤		
الاربعاء	٤	١١	١٨	٢٥		
الخميس	٥	١٢	١٩	٢٦		
الجمعة	٦	١٣	٢٠	٢٧		

تموز 7		محرم ١ـ صفر٢				
الأسبوع		العطلة الصيفية والتدريب الصيفي للمتدربين				
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الأحد		٦	١٣	٢٠	٢٧	
الاثنين		٧	١٤	٢١	٢٨	
الثلاثاء	١	٨	١٥	٢٢	٢٩	
الاربعاء	٢	٩	١٦	٢٣	٣٠	
الخميس	٣	١٠	١٧	٢٤	٣١	
الجمعة	٤	١١	١٨	٢٥		

آب 8		صفر٢ـ ربيع الأول ٣				
الأسبوع		العطلة الصيفية والتدريب الصيفي للمتدربين				
السبت	٣٠	٢	٩	١٦	٢٣	
الأحد	٣١	٣	١٠	١٧	٢٤	
الاثنين		٤	١١	١٨	٢٥	
الثلاثاء		٥	١٢	١٩	٢٦	
الاربعاء		٦	١٣	٢٠	٢٧	
الخميس		٧	١٤	٢١	٢٨	
الجمعة	١	٨	١٥	٢٢	٢٩	

العطل والمناسبات

٩/١٥ المولد النبوي الشريف (١٢ ربيع الأول)	٥/١ يوم العمال
١٠/٣ اليوم الوطني العراقي	٦/٥ يوم عرفة (٩ ذو الحجة)
١/١ رأس السنة الميلادية	٦/٦ـ٦/٩ عيد الأضحى (١٠ ـ ١٣ ذو الحجة)
١/٦ عيد الجيش	٦/٢٦ رأس السنة الهجرية ١٤٤٧هـ (١ محرم)
١/٢٧ ذكرى الإسراء والمعراج (٢٧ رجب)	٧/٥ يوم عاشوراء (١٠ محرم)
٣/٢٤ يوم الربيع	٩/١٤ ثورة ١٤ تموز
٣/٣٠ـ٤/١ عيد الفطر المبارك (١ ـ ٣ شوال)	جمعة او سبت او عطلة ◘ ، ذكرى او مناسبة ○

Chapter – 1

Introduction to Electronics

1-1: Physics of Semiconductors, Diodes and Transistors

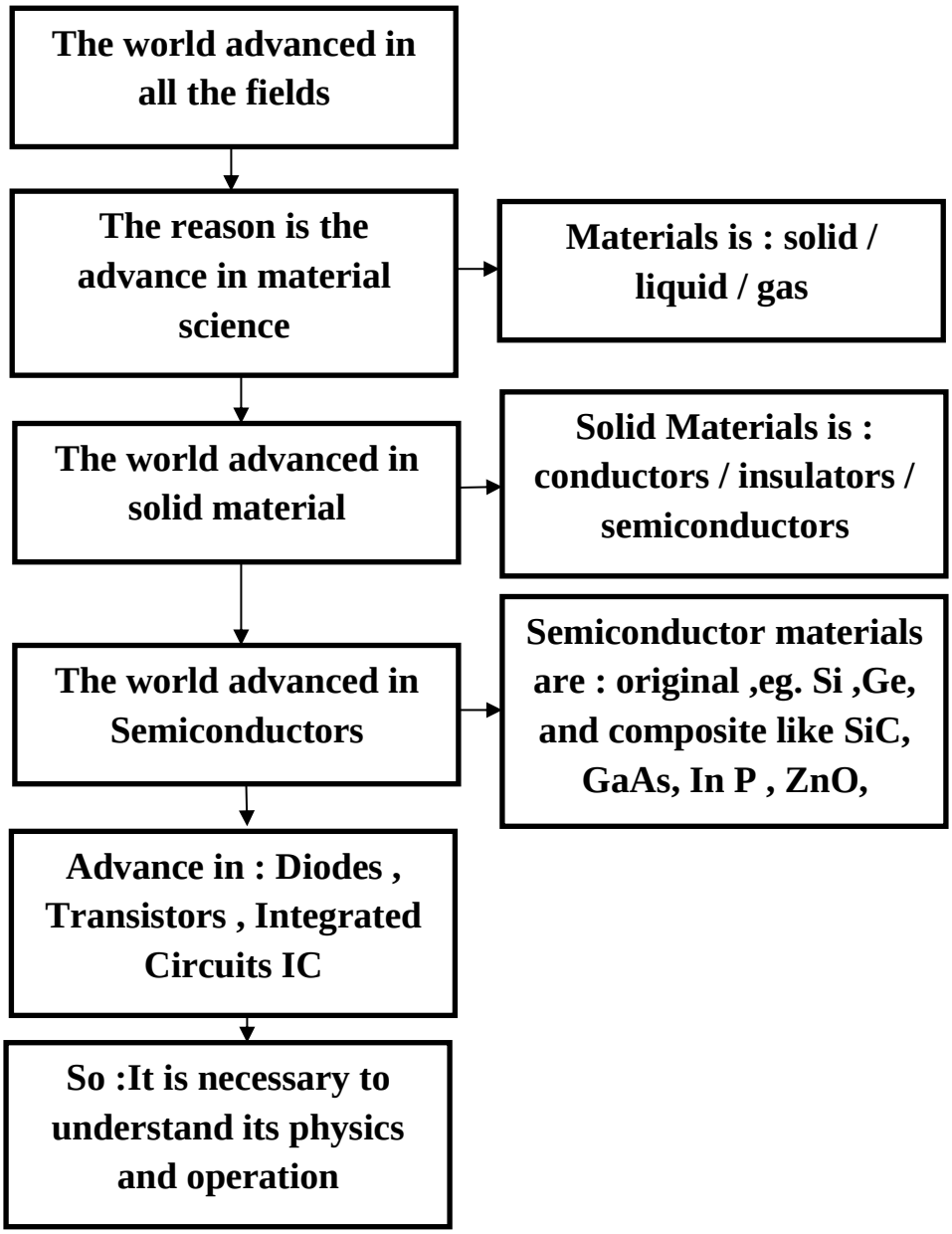


Fig.(1 – 1). The reasons of the Electronic advance

1-1-1: Silicon bond model: electrons and holes

Si is in Column IV of periodic table:

	IIIA	IVA	VA	VIA
	5 B	6 C	7 N	8 O
IIB	13 Al	14 Si	15 P	16 S
30 Zn	31 Ga	32 Ge	33 As	34 Se
48 Cd	49 In	50 Sn	51 Sb	52 Te

Fig.(1 – 2).Some of material groups of 2,3,4,5,6 groups

Electronic structure of Si atom:

- 10 core electrons (tightly bound)
- 4 valence electrons (loosely bound, responsible for most chemical properties)

Other semiconductors:

- Ge, C (diamond form), SiGe
- GaAs, InP, InGaAs, InGaAsP, ZnSe, CdTe (on average, 4 valence electrons per atom)

Silicon crystal structure:

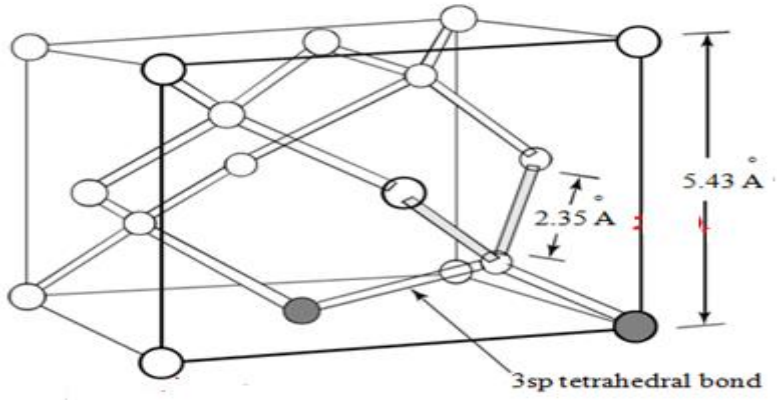


Fig.(1 – 3). Silicon crystal structure

- Silicon is a crystalline material:
  – long range atomic arrangement
- *Diamond* lattice:
  – atoms tetrahedrally bonded by sharing valence electrons (*covalent bonding*)
- Each atom shares 8 electrons:
  – low energy and stable situation

- Si atomic density: $5 \times 10^{22}\ cm^{-3}$

Simple ”flattened” model of Si crystal:

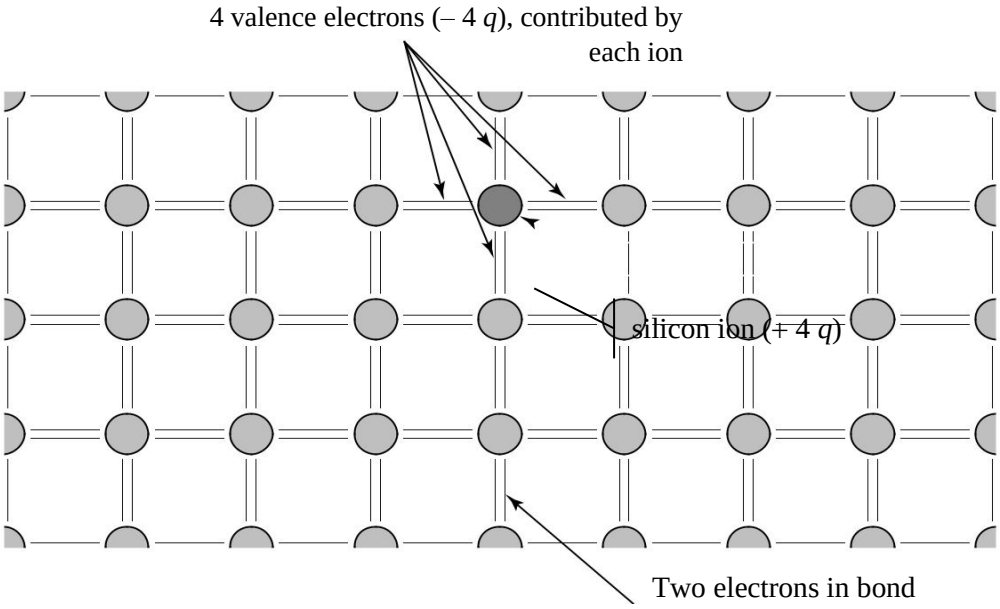


Fig.(1 – 4).sharing 4 electrons with covalent bonds

At 0º K :

- all bonds satisfied → all valence electrons engaged in bonding
- no ”free” electrons

At finite temperature:

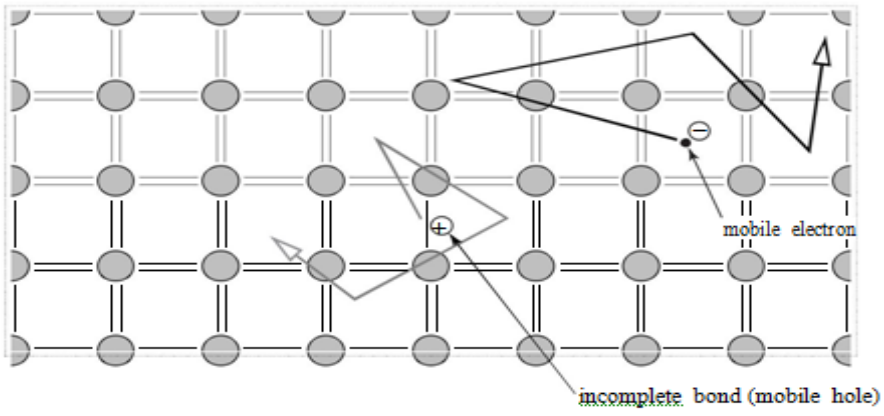


Fig.(1 –5).free electron and mobile hole

- finite thermal energy
- some bonds are broken
- ”free” electrons (mobile negative charge, $-1.6\times10^{-19}\ C$)
- ”free” *holes* (mobile positive charge, $1.6 \times 10^{-19}\ C$)

”Free” electrons and holes are called *carriers*:

• define:

$n \equiv$ (free) electron concentration $[cm^{-3}]$

$p \equiv$ hole concentration $[cm^{-3}]$

In thermal equilibrium and for a given semiconductor, np product is a constant that depends only on temperature!

1-1-2. Intrinsic semiconductor:

Question: In a perfectly pure semiconductor in thermal equilibrium at finite temperature, how many electrons and holes are there?

Since when a bond breaks, an electron *and* a hole are produced:

$$n_o = p_o$$

Also:

$$n_o p_o = n^2{}_i$$

Then:

$$n_o = p_o = n_i$$

$n_i \equiv$ *intrinsic* carrier concentration $[cm^{-3}]$

In Si at 300 K (”room temperature”): $n_i = 1\times 10^{10}\ cm^{-3}$

n_i very strong function of temperature: $T\uparrow \rightarrow n_i \uparrow$

1-1-3. Doping:

Introduction of foreign atoms to enhance semiconductor electrical properties.

A. Donors: introduce electrons to the semiconductor (but not holes)

- For Si, group-V atoms with 5 valence electrons (As, P, Sb)

	IIIA	IVA	VA	VIA
	5 B	6 C	7 N	8 O
IIB	13 Al	14 Si	15 P	16 S
30 Zn	31 Ga	32 Ge	33 As	34 Se
48 Cd	49 In	50 Sn	51 Sb	52 Te

Fig.(1 – 6).Some of Group 5 materials

- 4 electrons of donor atom participate in bonding
- 5th electron easy to release
  – at room temperature, each donor releases 1 electron that is available for conduction

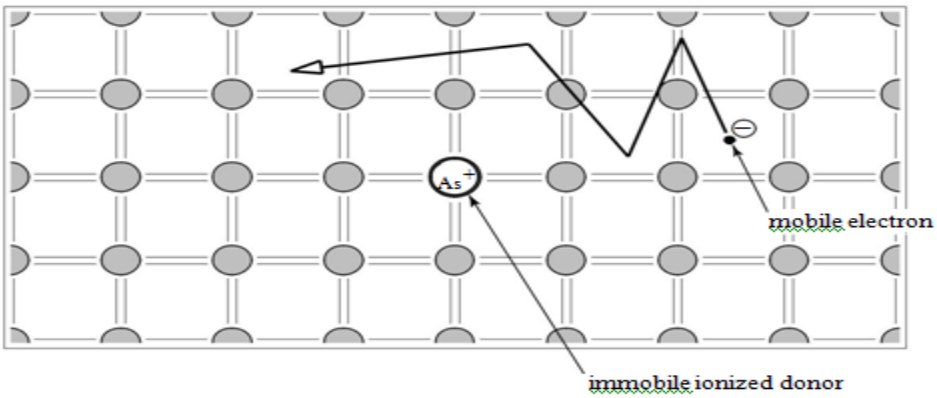


Fig.(1 –7).The free mobile electron of the donor

Define:

$N_d \equiv$ donor concentration [cm^{-3}]

(*intrinsic* semiconductor) $\rightarrow n_o = p_o = n_i$

• If $N_d >> n_i$, doping controls carrier concentrations (*extrinsic* semiconductor) $\rightarrow$

$$n_o = N_d \qquad p_o = \frac{n_i^2}{N_d}$$

Note: $n_o >> p_o$: *n -type semiconductor*

Example:

$N_d = 10^{17}\ cm^{-3} \rightarrow n_o = 10^{17}\ cm^{-3}$, $p_o = 10^3\ cm^{-3}$. In general: $N_d \sim 10^{15} - 10^{20}\ cm^{-3}$

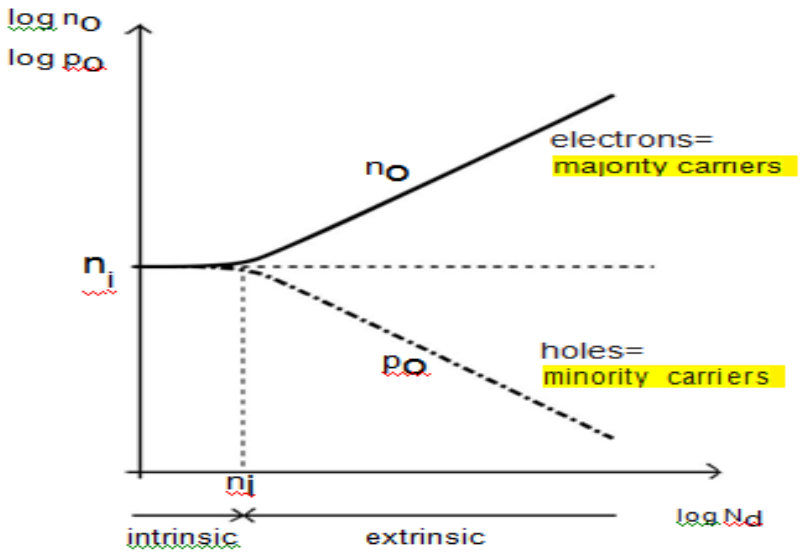


Fig.(1 – 8).The numbers of majority and minority carriers of N- type Si

B. Acceptors: introduce holes to the semiconductor (but not electrons)

• For Si, group-III atoms with 3 valence electrons (B: Boron)

	IIIA	IVA	VA	VIA
	5 B	6 C	7 N	8 O
IIB	13 Al	14 Si	15 P	16 S
30 Zn	31 Ga	32 Ge	33 As	34 Se
48 Cd	49 In	50 Sn	51 Sb	52 Te

Fig.(1 – 9).Some of Acceptor materials of group 3

- 3 electrons used in bonding to neighboring Si atoms
- 1 bonding site ”unsatisfied”:

– easy to ”accept” neighboring bonding electron to complete all bonds

– at room temperature, each acceptor releases 1 hole that is available to conduction

- acceptor site become negatively charged (fixed charge)

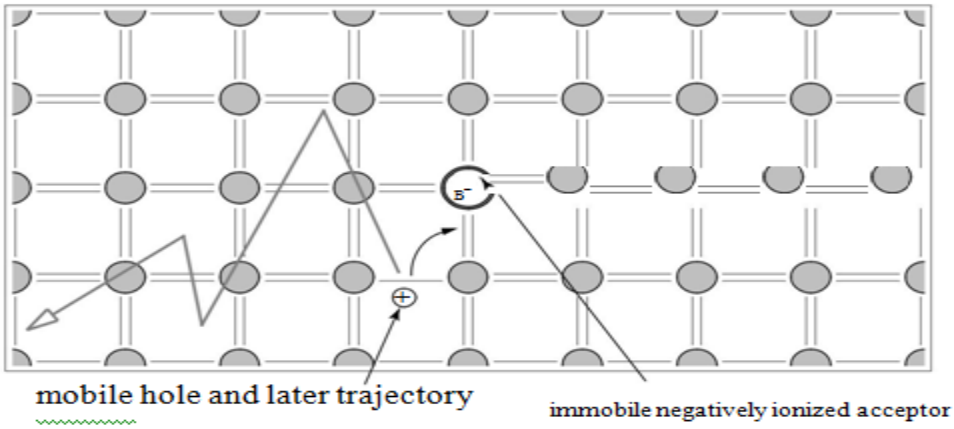


Fig.(1 – 10).The free hole of the acceptor

Define:

$N_a \equiv$ acceptor concentration $[cm^{-3}]$

• If $N_a \ll n_i$, doping irrelevant

(*intrinsic* semiconductor) $\rightarrow n_o = p_o = n_i$

• If N_a >> n_i, doping controls carrier concentrations (*extrinsic* semiconductor) →

$$p_o = N_a \qquad n_o = \frac{n_i^2}{N_a}$$

Note: p_o >> n_o: *p-type semiconductor*
Example:
$N_a = 10^{16}\ cm^{-3} \rightarrow p_o = 10^{16}\ cm^{-3}$, $n_o = 10^4\ cm^{-3}$.
In general: $N_a \sim 10^{15} - 10^{20}\ cm^{-3}$

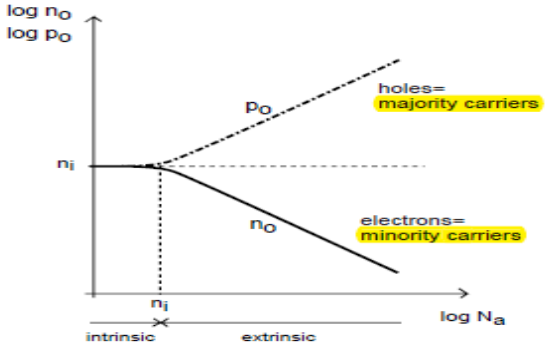


Fig.(1 – 11). The numbers of majority and minority carriers of P- type Si

Summary:

- In a semiconductor, there are two types of ”carriers”: electrons and holes
- In thermal equilibrium and for a given semiconductor $n_o p_o$ is a constant that only depends on temperature:

$$n_o p_o = n^2_i$$

• For Si at room temperature:

$$n_i \cong 10^{10}\ cm^{-3}$$

• *Intrinsic semiconductor*: ”pure” semiconductor.

$$n_o = p_o = n_i$$

- Carrier concentrations can be engineered by addition of ”dopants” (selected foreign atoms):

– n-type semiconductor:

$$n_o = N_d, \qquad p_o = \frac{n_i^2}{N_d}$$

– p-type semiconductor:

$$p_o = N_a, \qquad n_o = \frac{n_i^2}{N_a}$$

Review Questions:

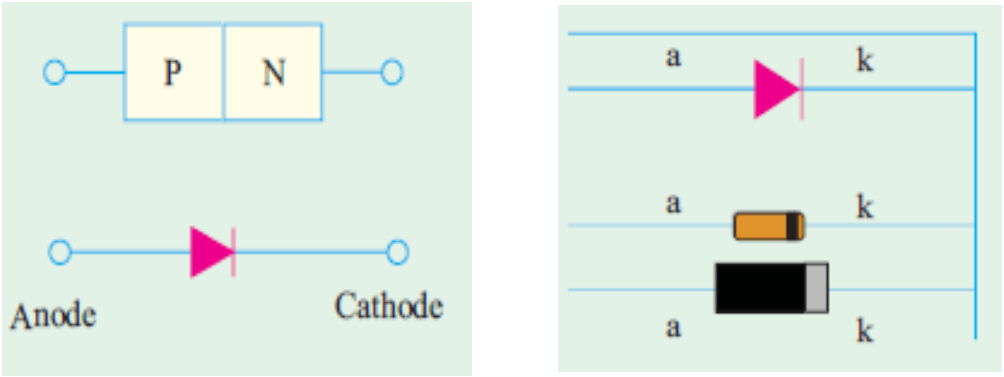
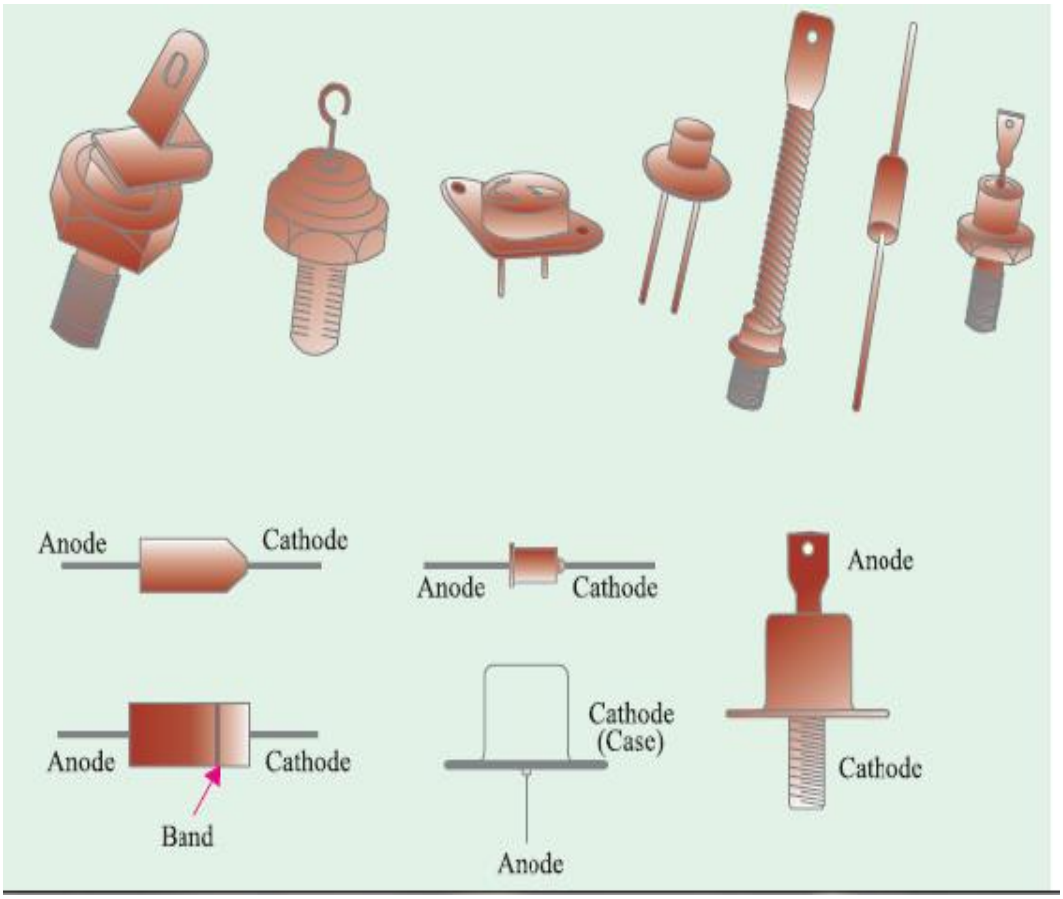
- How do semiconductors conduct electricity?
- What is a ”hole”?
- How many electrons and holes are there in a semiconductor in thermal equilibrium at a certain temperature?
- How can one enhance the conductivity of semiconductors?

1-2: Diode and its Equivalent Circuits:

1-2-1: Diode Notation:

Table (1-1) shows the diode notation and the image of the practical diodes.

Table (1-1).Diode notation and the image of few practical diodes

Diode notation	
Commercial junction diodes	

1-2-2: Ideal Diode :

In general, it is relatively simple to determine whether a diode is in the region of conduction or non-conduction simply by noting the direction of the current I_D established by an applied voltage. For conventional flow (opposite to that of electron flow), if the resultant diode current has the same direction as the arrowhead of the diode symbol, the diode is operating in the conducting region as depicted in Fig. 1.12a. If the resulting current has the opposite direction, as shown in Fig. 1.12 b, the open-circuit equivalent is appropriate.

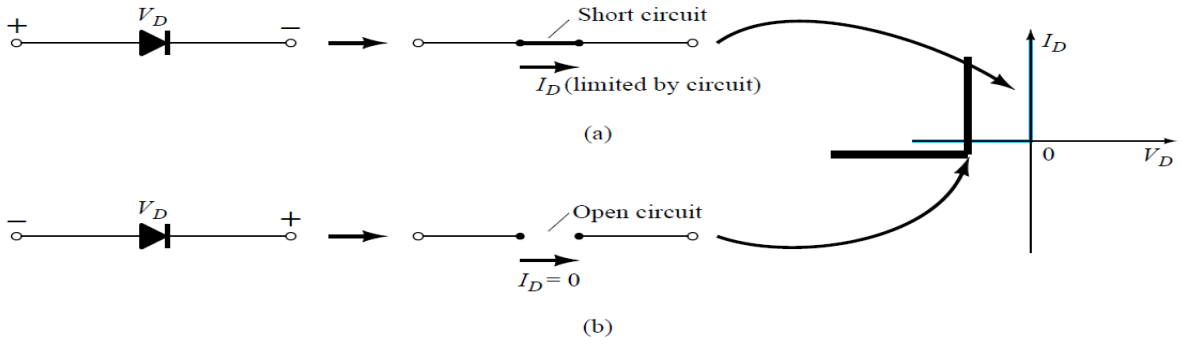
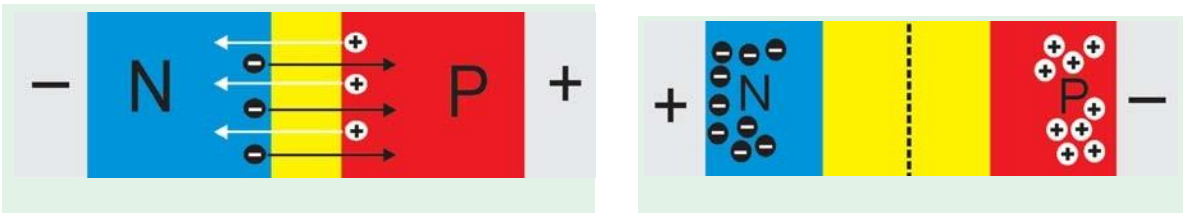


Figure 1.12 (a) Conduction and (b) nonconduction states of the ideal diode

1-2-3: V / I characteristics of the Diode :

1. Forward biase:

When the diode is forward-biased and the applied voltage is increased from zero, hardly any current flows through the device in the beginning. It is so because the external voltage is being opposed by the internal barrier voltage V_B whose value is **0.7 V for Si and 0.3 V for Ge**. As soon as V_B is neutralized, current through the diode increases rapidly with increasing applied battery voltage. It is found that as little a voltage as 1.0 V produces a forward current of about 50 mA. A burnout is likely to occur if forward voltage is increased beyond a certain safe limit, fig.(1.13a).



(a) (b)

Figure 1.13 (a) Forward Bias and (b) Reverse Bias

2. Reverse biase:

When the diode is reverse-biased, majority carriers are blocked and only a small current (due to minority carriers) flows through the diode. As the reverse voltage is increased from zero, the reverse current very quickly reaches its maximum or saturation value I_0 which is also known as ***leakage current***. It is of the order of nanoamperes (nA) for Si and microamperes

(μA) for Ge. The value of I_0 (or I_S) is independent of the applied reverse voltage but depends on ***(a)*** temperature, ***(b)*** degree of doping and ***(c)*** physical size of the junction.

Fig. 1.14 shows the static voltage-current characteristics for a low-power P-N junction diode.

As seen from Fig. 1.14, when reverse voltage exceeds a certain value called break-down voltage V_{BR} (or Zener voltage V_Z), the leakage current suddenly and sharply increases, the curve indicating zero resistance at this point. Any further increase in voltage is likely to produce burnout unless protected by a current-limiting resistor.

When P-N junction diodes are employed primarily because of this breakdown property as voltage regulators, they are called **Zener diodes** .

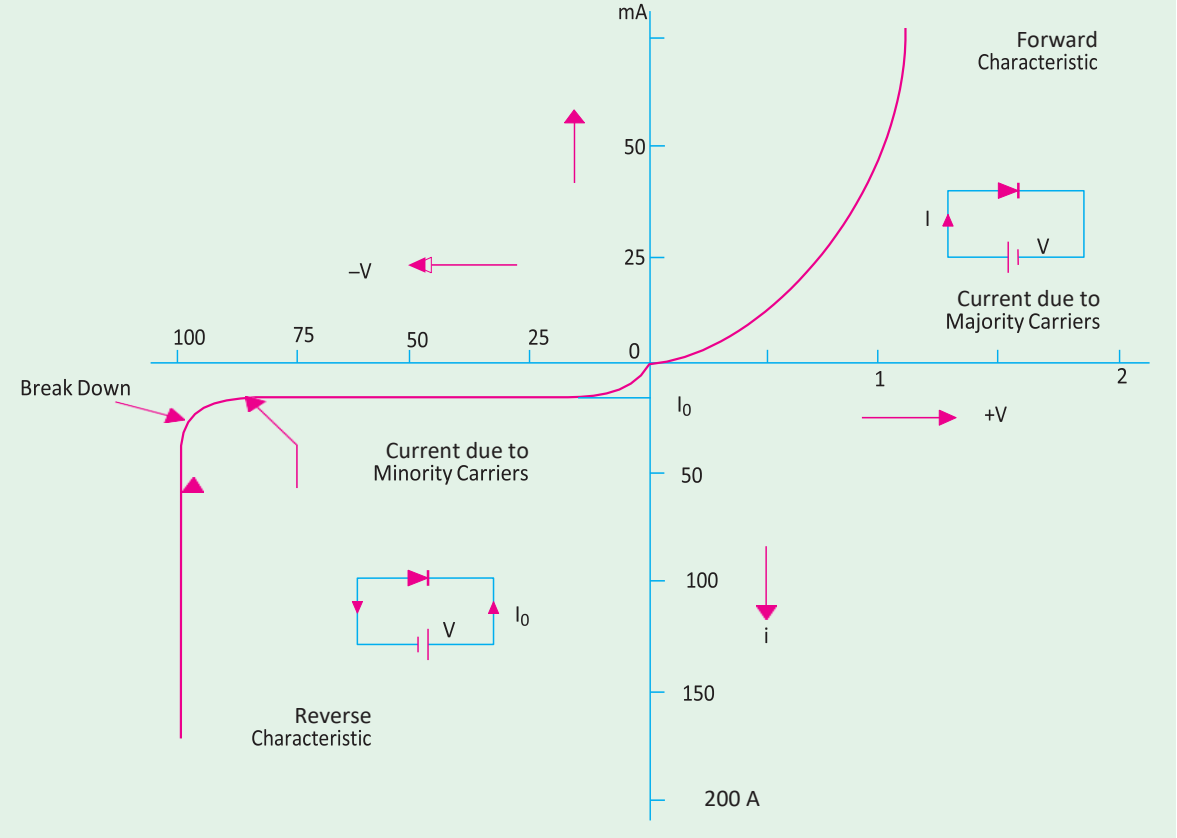


Fig 1.14 Static Voltage-Current characteristics for a low-power P-N junction diode.

1. Equation of the Static Characteristic

The volt-ampere characteristics described above are called ***static*** characteristics because they describe the d.c. behavior of the diode. The forward and reverse characteristics have been combined into a single diagram of Fig. 1.14.

These characteristics can be described by the analytical equation called ***Boltzmann diode equation***.

$$I = I_0 \left(e^{\frac{eV}{kT}} - 1\right) \text{ ampere}$$

where I_0 = diode reverse saturation current

V = voltage across junction – positive for forward bias and negative for reverse bias.

k = Boltzmann constant = 1.38×10^{-23} J/°K

T = crystal temperature in °K

η = 1 – for germanium

= 2 – for silicon

Hence, the above diode equation becomes

$I = I_0 (e^{eV/kT} - 1)$. – for germanium

$I = I_0 (e^{eV/2kT} - 1)$ – for silicon

Now, $e/k = 11{,}600$ and putting $T/11{,}600 = V_T$, the above equation may be written as

$$I = I_0 (e^{11{,}600V/\eta T} - 1) = I_0 (e^{V/\eta V_T} - 1) \text{ ampere}$$

Now, at room temperature of (273 + 20) = 293°K, $V_T = 293/11{,}600 = 0.025$ V = 25 mV. Substituting the value of η, we have

$I = I_0 (e^{40V} - 1)$ – for Ge

$\cong I_0 e^{40V}$ – if $V > 1$ volt

$I = I_0 (e^{20V} - 1)$ – for Si

$\cong I_0 e^{20V}$ – if $V > 1$ volt

We may also write the above diode equation as under

$I = I_0 (e^{V_f/\eta V_T} - 1)$ – forward bias

$= I_0 (e^{V_R/\eta V_T} - 1)$ – reverse bias

Example 52.1. *Using approximate Boltzmann's diode equation, find the change in forward bias for doubling the forward current of a germanium semiconductors at 290°K.*

(Basic Electronics, Osmania Univ. 1993)

Solution. The approximate Boltzmann's diode equation is given by $I = I_0 \exp(eV/kT)$

$\therefore \quad I_1 = I_0 \exp(eV_1/kT)$ and $I_2 = I_0 \exp(eV_2/kT)$

$\therefore \quad \frac{I_2}{I_1} = \exp\left[\frac{e}{kT}(V_2 - V_1)\right]$

or $\quad (V_2 - V_1) = \frac{kT}{e} \ln\left(\frac{I_2}{I_1}\right) = 25 \ln\left(\frac{I_2}{I_1}\right)$ mV

Since $\quad I_2 = 2I_1$ or $I_2 / I_1 = 2$

$\therefore \quad (V_2 - V_1) = 25 \ln 2 = 25 \times 0.693 =$ **17.3 mV**

Example 52.5. *Find the current through the 20 Ω resistor shown in Fig. 52.6 (a). Each silicon diode has a barrier potential of 0.7 V and a dynamic resistance of 2 Ω. Use the diode equivalent circuit technique.* **(Semiconductor Devices, Gujarat BTE, 1993)**

Solution. In Fig. 52.6 (*b*) each diode has been replaced by its equivalent circuit. It is seen that diodes D_1 and D_3 are forward-biased by 5 V battery whereas D_2 and D_4 are reverse-biased. Hence, the current will flow from point *A* to *B*, then to *C* via 20 Ω resistance and then back to the negative terminal of the 5 V battery.

The net voltage in the equivalent circuit is

$$V_{net} = 5 - 0.7 - 0.7 = 3.6 \text{ V}$$

Total resistance seen by this net voltage is

$$R_T = 2 + 20 + 2 = 24\ \Omega$$

The circuit current $I = V_{net}/R_T = 3.6/24 = \mathbf{0.15\ A}$

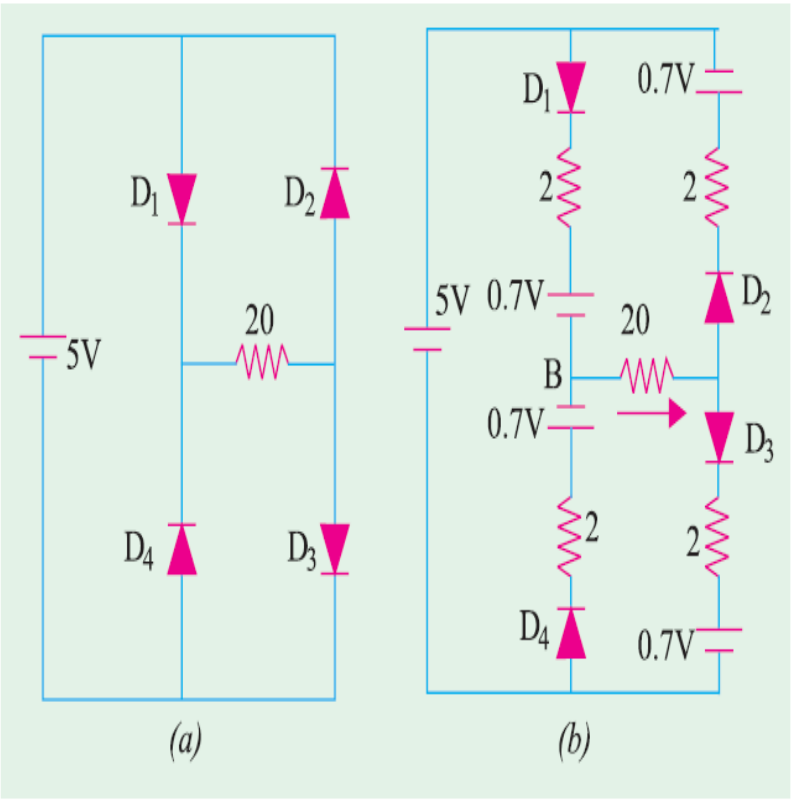


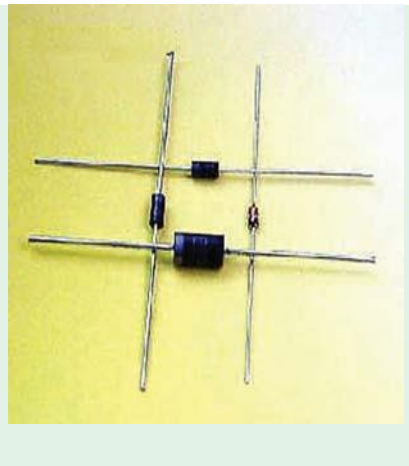
Fig. 52.6

1.2.4: Junction Breakdown :

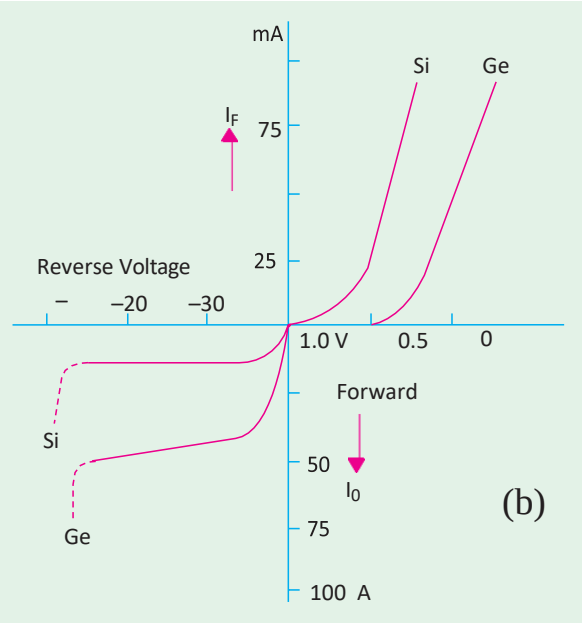
If the reverse bias applied to a *P-N* junction is increased, a point is reached when the junction breaks down and reverse current rises sharply to a value limited only by the external resistance connected in series with the junction (Fig. 1.15).

This critical value of the voltage is known as **breakdown voltage** (V_{BR}). It is found that once breakdown has occurred, very little further increase in voltage is required to increase the current to relatively high values. The junction itself offers almost zero resistance at this point.

The breakdown voltage depends on the width of the depletion region which, in turn, depends on the doping level.



(a)



(b)

Fig. (1-15).(a) Zener Diodes,(b) Break down of the diode

The following two mechanism are responsible for breakdown under increasing reverse voltage:

1. Zener Breakdown

This form of breakdown occurs in junctions which, being heavily doped, have narrow depletion layers. The breakdown voltage sets up a very strong electric field (about 10^8 V/m) across this narrow layer. This field is strong enough to ***break or rupture the covalent bonds*** thereby generating electron-hole pairs. Even a small further increase in reverse voltage is capable of producing large number of current carriers. That is why the junction has very low resistance in the break-down region.

2. Avalanche Breakdown

This form of breakdown occurs in junctions which being lightly-doped, have wide depletion layers where the electric field is not strong enough to produce Zener breakdown. Instead, the minority carriers (accelerated by this field) collide with the semiconductor atoms in the depletion region. Upon collision with valence electrons, covalent bonds are broken and electron-hole pairs are generated. These newly-generated charge carriers are also accelerated by the electric field resulting in more collisions and hence further production of charge carriers. This leads to an avalanche (or flood) of charge carriers and, consequently, to a very low reverse resistance. The two breakdown phenomena are shown in Fig. 1.15.

1-2-5: Approximate Diode Circuit Solutions

There is often a need for us to perform design with pencil and paper. Remember: simulation packages don't design for you, they only analyze circuits. There's a big difference between design and analysis!

There are two very important approximate diode models that allow easier paper designs:

a). Constant-Voltage-Drop (CVD) Model.
b). Piecewise Linear (PWL) Model.

a). Constant-Voltage-Drop (CVD) Model

In this model, the characteristic curve is approximated as:

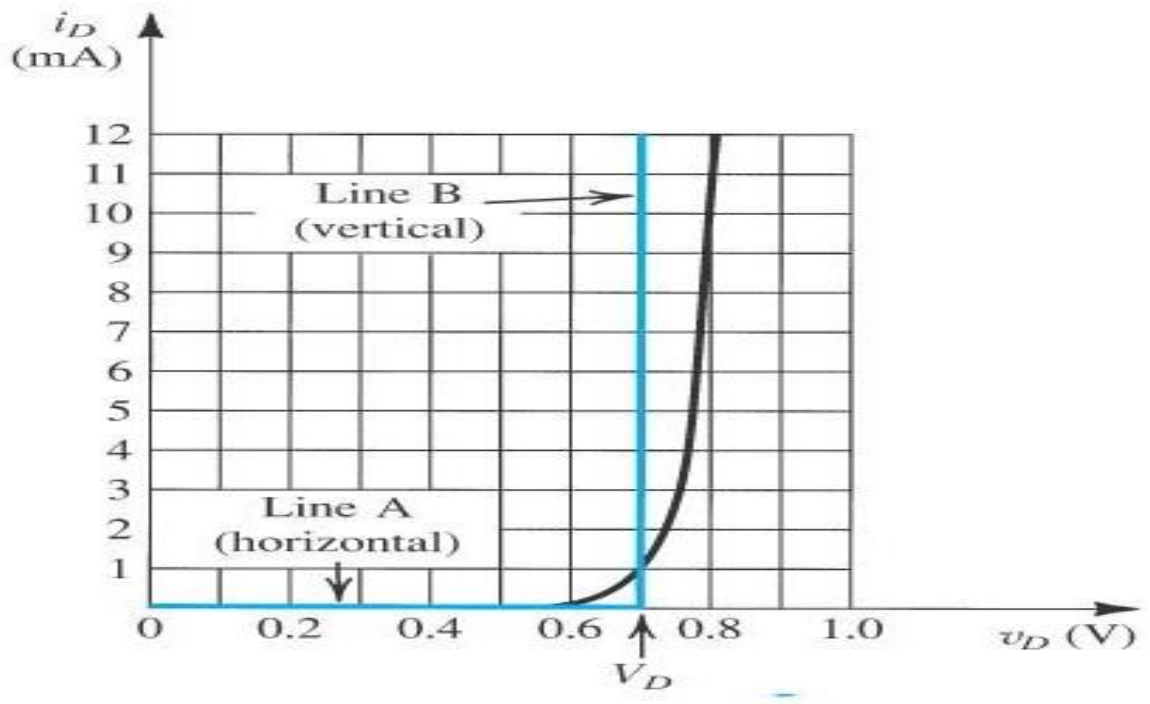


Fig. (1-16).The diode characteristics of CVD model

In words, this model says that if the diode is forward biased, then the voltage drop across the diode is V_D. If not forward biased, the diode is then reversed biased and the current is zero and VD can be any value < V_D.

V_D is often set to 0.7 V for silicon diodes, as shown above, while set to 0.2 V for Schottky diodes, for example.

The CVD circuit model for diodes is

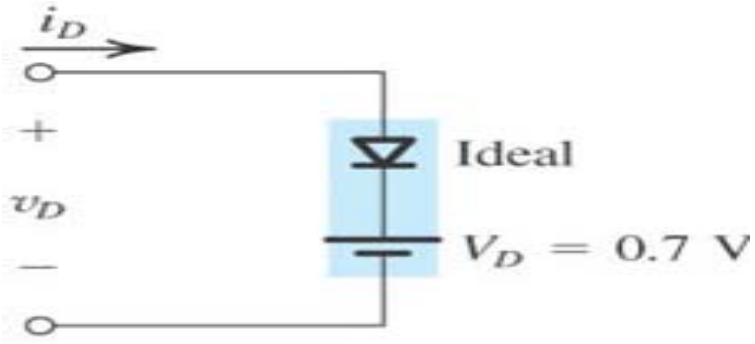


Fig.(1-17). The CVD circuit model for the diode.

This is probably the most commonly used diode model for hand calculations.

Example N1.1. Determine the current *I* in the circuit below using the CVD model and assuming a silicon diode.

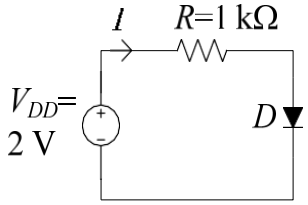


Fig.(1-18).

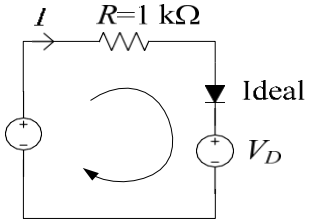


Fig.(1-19).

Using the CVD model of Fig.(1-18) the equivalent approximate circuit is shown in fig.(1-19): Assuming the diode is forward conducting (i.e., "on") with V_D = 0.7 V and using KVL (Kirchhoff's Voltage Law)in this circuit :

$$2 = IR + V_D$$

Or: $$I = (2 - V_D)/R = (2 - 0.7)/1000 = 1.3\ mA$$

The positive value of this current indicates our original assumption that the diode is "on" is correct.

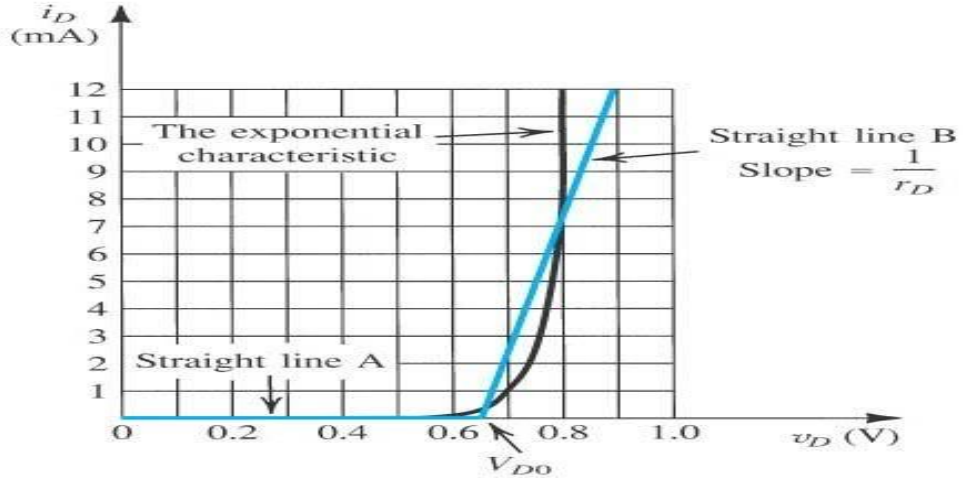
What is the value of *I* if V_{DD} = 0.5 V? By KVL again,

$$I = (0.5 - V_D)/R = (0.5 - 0.7)/1000 = -0.2\ mA$$

Since *I* is negative, then D must be reversed biased. This means our initial forward conducting assumption was incorrect. Rather, in this situation *I* = 0 and V_D = 0.5 V.

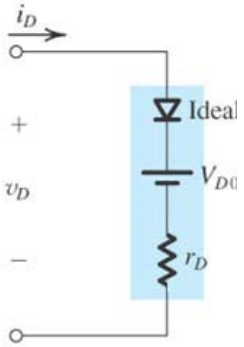
b).Piecewise Linear (PWL) Diode Model

This is a "battery plus internal diode resistance model." It is one step better than the CVD model by incorporating a slope to the interpolative line:



(Fig. 1-20).The I-V characteristics of the diode

The finite slope to this curve (Fig. 1-17) means that the diode has a non- zero internal resistance, which we will label as r_D. The equivalent circuit for the PWL diode model is as shown in fig.(1-18).



(Fig. 1-21). The equivalent circuit for the PWL diode model

Example N1.2. Determine the current I in the circuit below using the PWL diode model shown in Fig. (1-22).

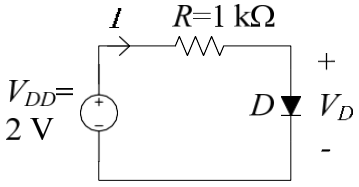


Fig. (1-22).

From Fig. (1-22), we can determine V_{D0} and r_D for the particular diode whose characteristic equation is shown:

- V_{D0} = 0.65 V
- $r_D = run/rise$ = (0.9 – 0.65) / 12 x 10^{-3} = 20.8 Ω

The equivalent circuit using the PWL model of the diode is then as shown in fig.(1-23).

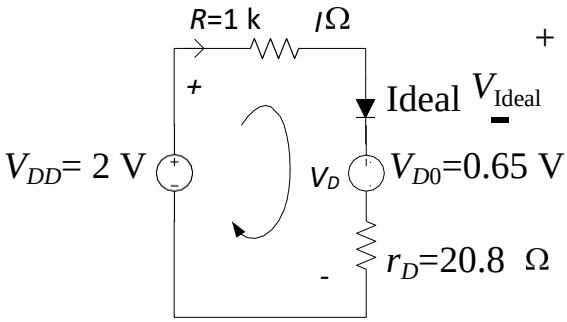


Fig. (1-23).

Assuming the diode is "on,", then by KVL:

$$2 = I \text{ x}1000 + 0.65 + 20.8\text{x } I$$

or $$I = 1.32 \text{ mA}.$$

This is close to the 1.3 mA we computed in the last example using the cruder CVD model. Again, the positive value of this current indicates that we made the correct choice that the diode is "on."

What's the forward voltage drop across the diode?

$$V_D = 2 - 1000 \text{ x } 1.32\text{x}10^{-3} = 0.68 \text{ V}$$

Is this enough to turn the diode on? Yes, referring to the equivalent circuit above.

$$V_{Ideal} = V_D - 0.65 - 20.8 \text{ x } 1.32\text{x}10^{-3} \cong 0^+ \text{ V}$$

1-2-6: Applications:

1. **Rectifier Circuits**
2. **Conversions of AC to DC for DC operated circuits**
3. **Battery Charging Circuits**
4. **Simple Diode Circuits**
5. **Protective Circuits against Over current, Polarity Reversal and Currents caused by an inductive kick in a relay circuit**
6. **Zener Circuits**
7. **Overvoltage Protection**
8. **Setting Reference Voltages**

Chapter – 2

Application of Diodes

2-1. Half Wave Rectifier (HWR):

Since diodes restrict the flow of current to one direction, they can be used to convert an AC power supply, which switches polarity from + to - many times a second, into a straight DC supply.

The simplest rectifier uses one diode, like this:

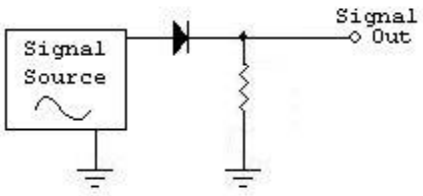


Fig.(2-1).Half- wave Rectifier

Called a *half-wave rectifier*, this circuit takes an AC signal in and chops off anything that falls below 0 Volts.

Signal In: Signal Out (Half-wave):

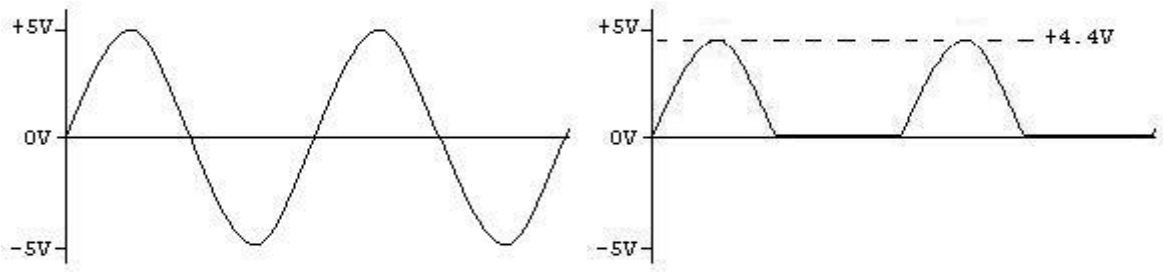


Fig.(2-2).The input and output waveforms of the HWR

The half-wave rectifier is used in AM radios to rectify the signal. But for a rectifier in a power supply, it leaves something to be desired -- we lose half the power! Luckily, we can do better.

2-2. Full Wave Rectifiers (FWR):

The circuits which convert the input alternating current (AC) into direct current (DC) are referred to as rectifiers. If such rectifiers rectify both the positive as well as negative pulses of the input waveform, then they are called Full-Wave Rectifiers. Figure (2-21) shows such a rectifier designed using a multiple winding transformer whose secondary winding is equally divided into two parts with a provision for the connection at its central point (and thus referred to as the centre-tapped transformer),

two diodes (D_1 and D_2) and a load resistor (R_L). Here the AC input is fed to the primary winding of the transformer while an arrangement of diodes and the load resistor which yields the DC output, is made across its secondary terminals.

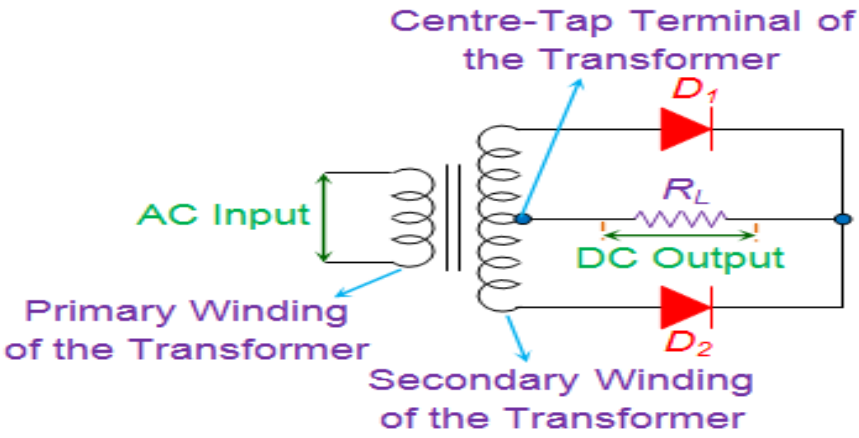


Fig. (2-3). Full-Wave Rectifier Circuit

The circuit can be analyzed by considering its working during the positive and the negative input pulses separately.

Figure (2-22 a) shows the case where the AC pulse is positive in nature i.e. the polarity at the top of the primary winding is positive while its bottom will be negative in polarity. This causes the top part of the secondary winding to acquire a positive charge while the common center-tap terminal of the transformer will become negative.

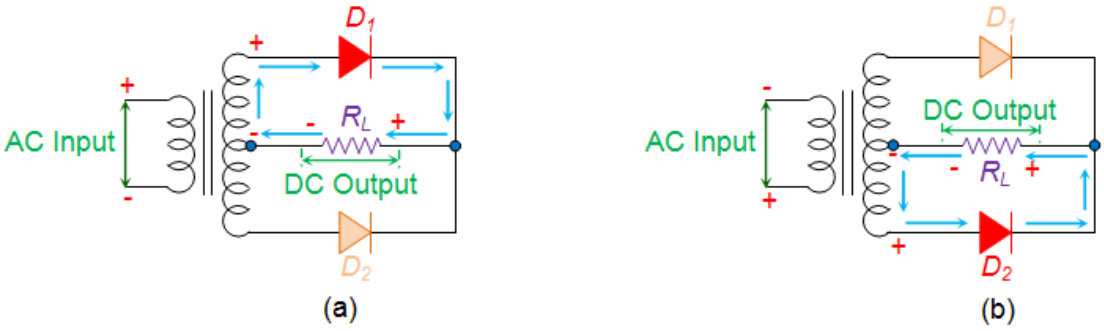


Fig.(2-4). Conduction path of Full-Wave Rectifier for (a) positive input pulse, (b) negative input pulse

This causes the diode D_1 to be forward biased which in turn causes the flow of current through R_L along the direction shown in Figure 2a. However, at the same time, diode D_2 will be reverse biased and hence acts like an open circuit. This causes the appearance of positive pulse across the R_L, which will be the DC output. Next, if the input pulse becomes negative in nature, then the top and the bottom of the primary winding will acquire the negative and the positive polarities respectively. This causes the bottom of the secondary winding to become positive while its center-tapped terminal will become negative. Thus, the diode D_2 gets forward biased while the D_1 will get reverse biased which allows the flow of current as shown in the Figure 2-22b.

Here the most important thing to note is the fact that the direction in which the current flows via R_L will be identical in either case (both for positive as well as for negative input pulses). Thus, we get the positive output pulse even for the case of negative input pulse (Figure 2-23), which indicates that both the half cycles of the input AC are rectified.

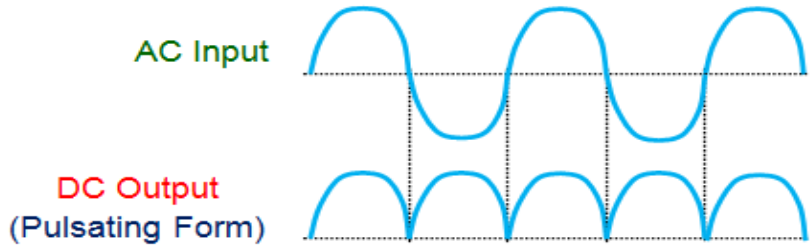


Fig. (2-5). input and output waveforms of the Full Wave Rectifier

Such circuits are referred to as:

(i) Centre-Tapped **Full Wave Rectifiers** as they use a centre-tapped transformer,

(ii) Two-Diode Full-Wave Rectifiers because of the use of two diodes and/or

(iii) Bi-Phase Circuits due to the fact that in these circuits, the output voltage will be the phasor addition of the voltages developed across the load resistor due to two individual diodes, where each of them conducts only for a particular half-cycle.

However as evident from Figure 2-23, the output of the rectifier is not pure DC but pulsating in nature, where the frequency of the output waveform is seen to be double of that at the input. In

order to smoothen this, one can connect a capacitor across the load resistor as shown by the Figure (2-24). This causes the capacitor to charge via the diode D_1 as long as the input positive pulse increases in its magnitude. By the time the input pulse reaches the positive maxima, the capacitor would have charged to the same magnitude. Next, as long as the input positive pulse keeps on decreasing, the capacitor tries to hold the charge acquired (being an energy-storage element).

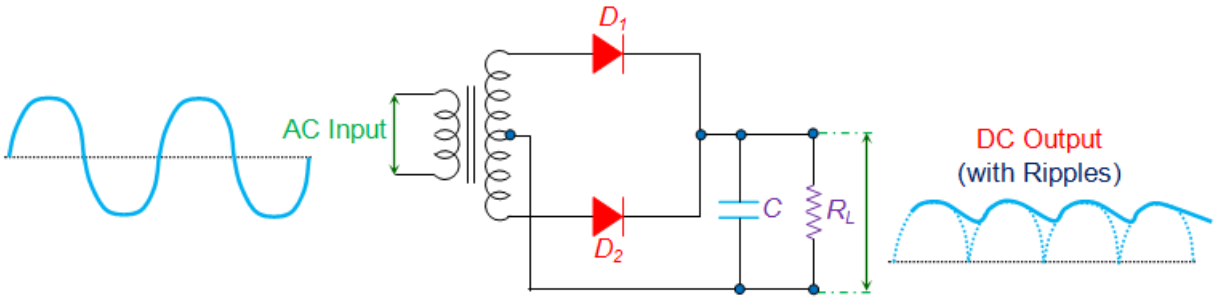


Fig. (2-6). Full Wave Rectifier with RC filter

However, there will be voltage-loss as some amount of charge gets lost through the path provided by the load resistor (nothing but discharging phenomenon). Further, as the input pulse starts to go low to reach the negative maxima, the capacitor again starts to charge via the path provided by the diode D_2 and acquires an almost equal voltage but with opposite polarity. Next, as the input voltage starts to move towards 0V, the capacitor slightly discharges via R_L. This charge-discharge cycle of the capacitor

causes the ripples to appear in the output waveform of the full-wave rectifier with RC filter as shown in Figure 2-24.

Further it is to be noted that the two-diode full-wave rectifier shown in Figure 2-21 is costly and bulky in size as it uses the complex center-tapped transformer in its design. Thus, one may resort to another type of full-wave rectifier called Full-Wave Bridge Rectifier (identical to Bridge Rectifier) It also offers high power applications. However it is to be noted that the full wave bridge rectifier uses four diodes instead of two.

The half-wave rectifier chopped off half our signal. A full-wave rectifier does more clever trick: it flips the - half of the signal up into the + range. When used in a power supply, the full-wave rectifier allows us to convert almost all the incoming AC power to DC. A full-wave rectifier uses a diode bridge, made of four diodes, like this(fig.2-25):

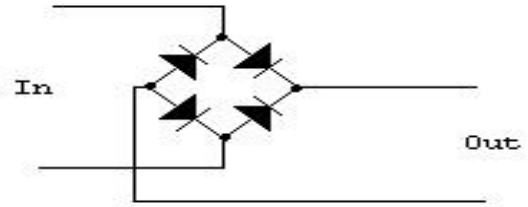


Fig. (2-7). Full-wave bridge rectifier

At first, this may look just as confusing as the one-way streets. The thing to realize is that the diodes work in pairs. As the voltage of the signal flips back and forth, the diodes let the current to always flow in the same direction for the output.
Here's what the circuit looks like (fig.2-8) to the signal as it alternates:

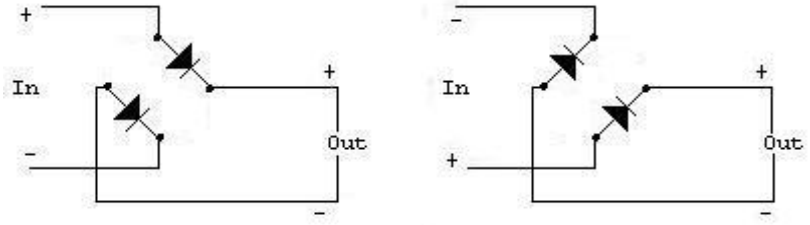


Fig. (2-8). Current flow for the positive and negative parts of the input signal

So, if we feed our AC signal into a full wave rectifier, we'll see both halves of the wave above 0 Volts. Since the signal passes through two diodes, the voltage out will be lower by two diode drops, or 1.2 Volts, (fig.2-9).

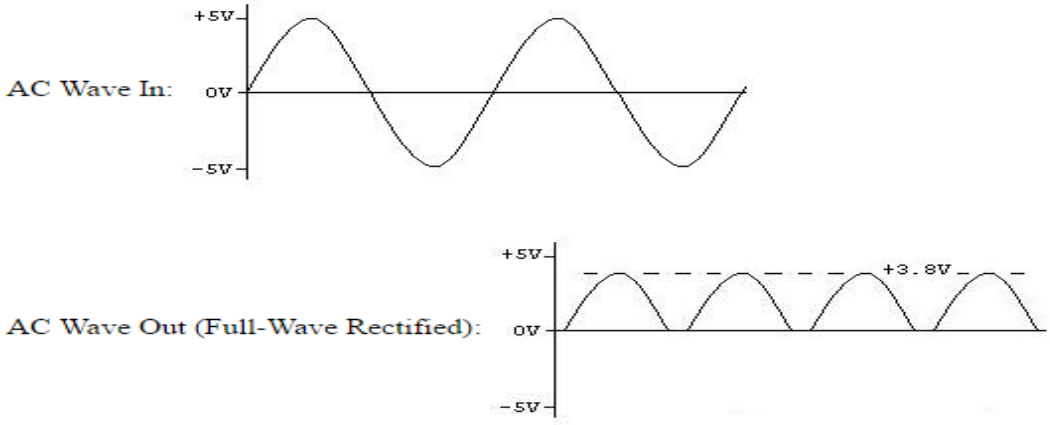


Fig. (2-9).Input and Output waveforms of the Bridge Rectifier

If we're interested in using the full-wave rectifier as a DC power supply, we'll add a smoothing capacitor to the output of the diode bridge.

More Examples on Rectifiers (From Boylestad)

EXAMPLE 2.18

(a) Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.48.
(b) Repeat part (a) if the ideal diode is replaced by a silicon diode.
(c) Repeat parts (a) and (b) if V_m is increased to 200 V and compare solutions using Eqs. (2.7) and (2.8).

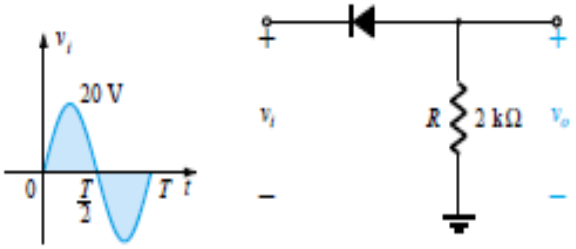


Figure 2.48 Network for Example 2.18.

Solution

(a) In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.49, and v_o will appear as shown in the same figure. For the full period, the dc level is

$$V_{dc} = -0.318V_m = -0.318(20\text{ V}) = \mathbf{-6.36\text{ V}}$$

The negative sign indicates that the polarity of the output is opposite to the defined polarity of Fig. 2.48.

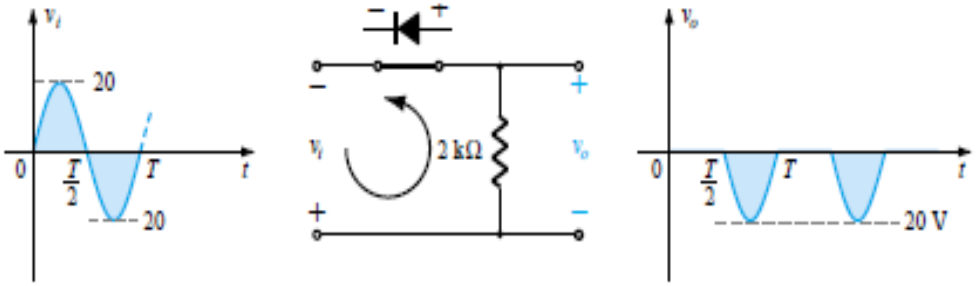


Figure 2.49 Resulting v_o for the circuit of Example 2.18.

(b) Using a silicon diode, the output has the appearance of Fig. 2.50 and

$$V_{dc} \cong -0.318(V_m - 0.7\text{ V}) = -0.318(19.3\text{ V}) \cong \mathbf{-6.14\text{ V}}$$

The resulting drop in dc level is 0.22 V or about 3.5%.

(c) Eq. (2.7): $V_{dc} = -0.318V_m = -0.318(200\text{ V}) = \mathbf{-63.6\text{ V}}$

Eq. (2.8): $V_{dc} = -0.318(V_m - V_T) = -0.318(200\text{ V} - 0.7\text{ V})$

$= -(0.318)(199.3\text{ V}) = \mathbf{-63.38\text{ V}}$

which is a difference that can certainly be ignored for most applications. For part c the offset and drop in amplitude due to V_T would not be discernible on a typical oscilloscope if the full pattern is displayed.

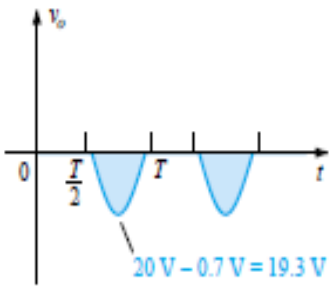


Figure 2.50 Effect of V_T on output of Fig. 2.49.

Determine the output waveform for the network of Fig. 2.63 and calculate the output dc level and the required PIV of each diode.

EXAMPLE 2.19

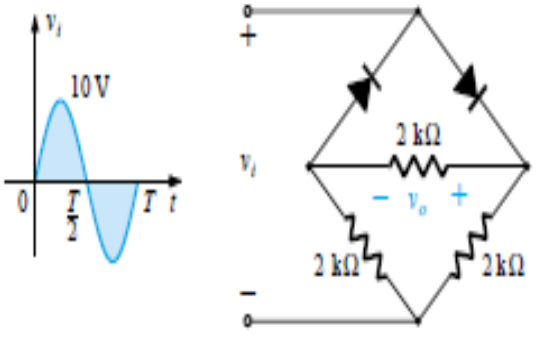


Figure 2.63 Bridge network for Example 2.19.

Solution

The network will appear as shown in Fig. 2.64 for the positive region of the input voltage. Redrawing the network will result in the configuration of Fig. 2.65, where $v_o = \frac{1}{2}v_i$ or $V_{o_{max}} = \frac{1}{2}V_{i_{max}} = \frac{1}{2}(10\text{ V}) = 5\text{ V}$, as shown in Fig. 2.65. For the negative part of the input the roles of the diodes will be interchanged and v_o will appear as shown in Fig. 2.66.

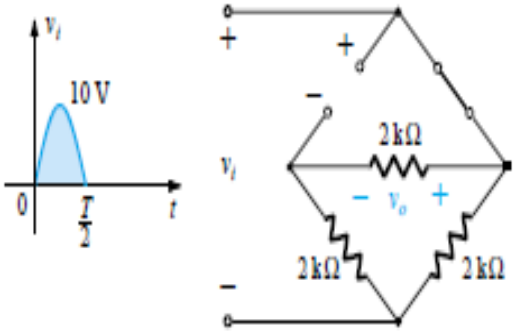


Figure 2.64 Network of Fig. 2.63 for the positive region of v_i.

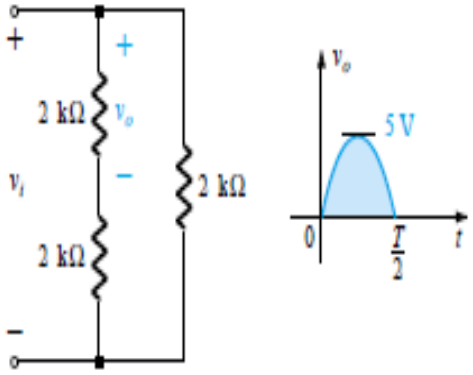


Figure 2.65 Redrawn network of Fig. 2.64.

The effect of removing two diodes from the bridge configuration was therefore to reduce the available dc level to the following:

$$V_{dc} = 0.636(5\text{ V}) = 3.18\text{ V}$$

or that available from a half-wave rectifier with the same input. However, the PIV as determined from Fig. 2.58 is equal to the maximum voltage across R, which is 5 V or half of that required for a half-wave rectifier with the same input.

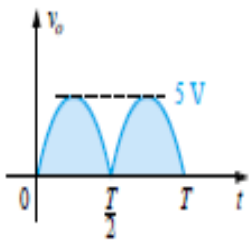


Figure 2.66 Resulting output for Example 2.19.

2-3: Diode Limiters (Clippers):

1. Basic Description

As you know, diodes can be used as switches depending on the biasing type, reverse or forward fig.2-10). The clipping circuit, also referred to as clipper, clips off some of the portions of the input signal and uses the clipped signal as the output signal. The clamping circuit or clamper keeps the amplitude of the output signal same as that of the input signal except that the D.C. level (offset) has been changed. The clamper through which the input waveform shifts to positive direction is called positive clamper, otherwise, is called **negative clamper**.

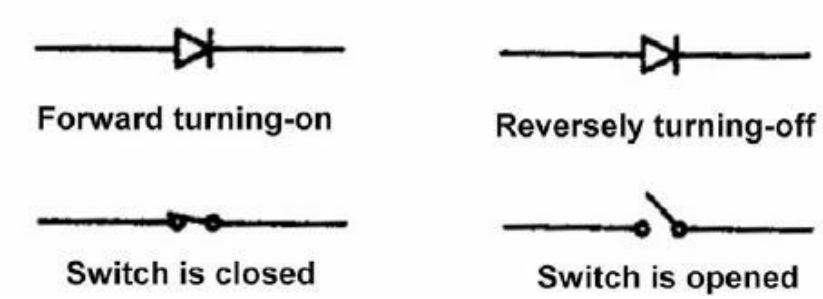


Fig. 2.10 – Ideal Diode – Switch Terminology

2. Clipper Circuits

There are two types of clipper circuits, the series and parallel diode clipping circuits.

2-a).Series Diode Clipping Circuit

In these type of circuits, the diode is connected between the input and output voltage terminals (**Fig 2.11**)

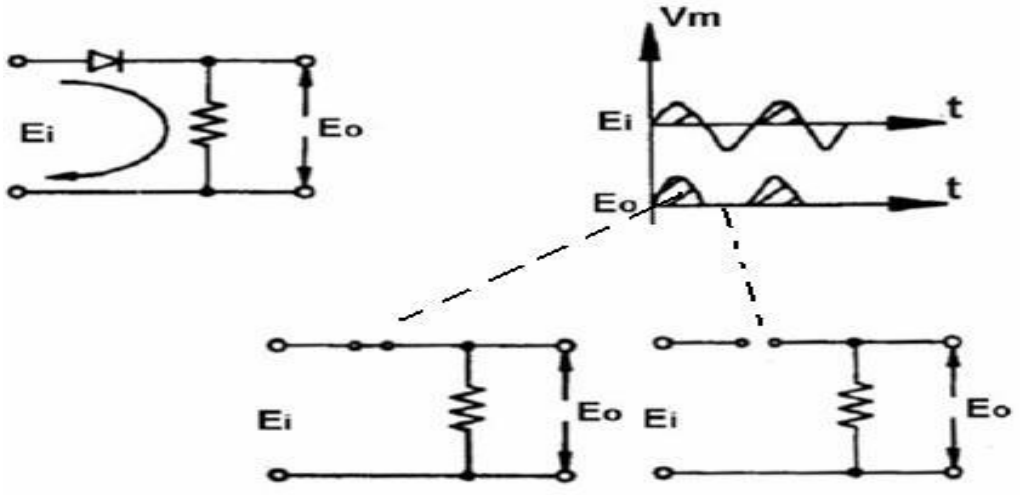


Fig. 2.11. Negative Clipping circuit.

As **Fig.2.11** reveals, the negative cycle of the input voltage can be clipped of by this type of series clippers. Reverse of the diode pins yields to a positive cycle clipping circuit as shown in **Fig. 2.12**.

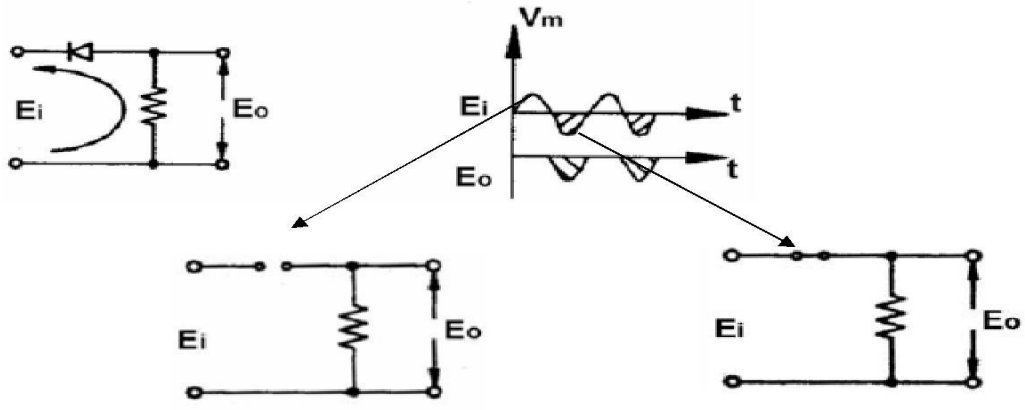
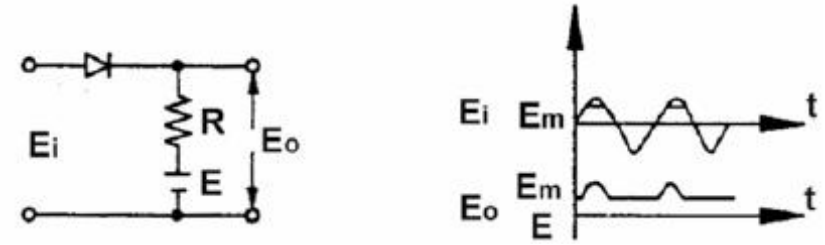


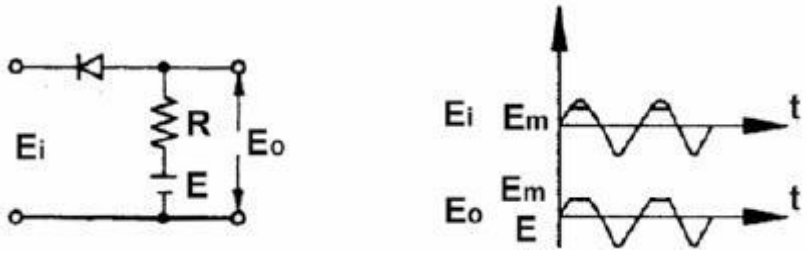
Fig. 2.12. Positive Clipping circuit.

Previous circuits clip the values larger or smaller than zero voltage. This voltage, technically called **"threshold voltage"** and can be changed to a desired value by inserting a D.C. voltage source. This is achieved in two different ways.

In the first type, the voltage source of $\mathbf{E_m}$ (positive or negative) is connected through output terminals as in **Fig. 2.13.** Depending on the diode connection (normal or reverse), the values smaller **(Fig.2.13.a)** or greater **(Fig.2.13.b)** than $\mathbf{E_m}$ is clipped and assigned as E_m. .



a



b

Fig. 2.13. First type of Threshold Series Clipping Circuit

Note that if $\mathbf{E_m}$ is negative, (where the voltage source is reversely connected) again the values smaller or larger than this negative value is clipped, do not get confused.

In the second type of threshold series clipping (fig.2-14), the voltage source is applied between the input and output terminals, series with the diode. This time, the clipped values are assigned to zero and the net output voltage equals to the difference between the input and threshold values.

(If E_m is negative, then: $E_0 = E - E_m = E + |E_m|$)

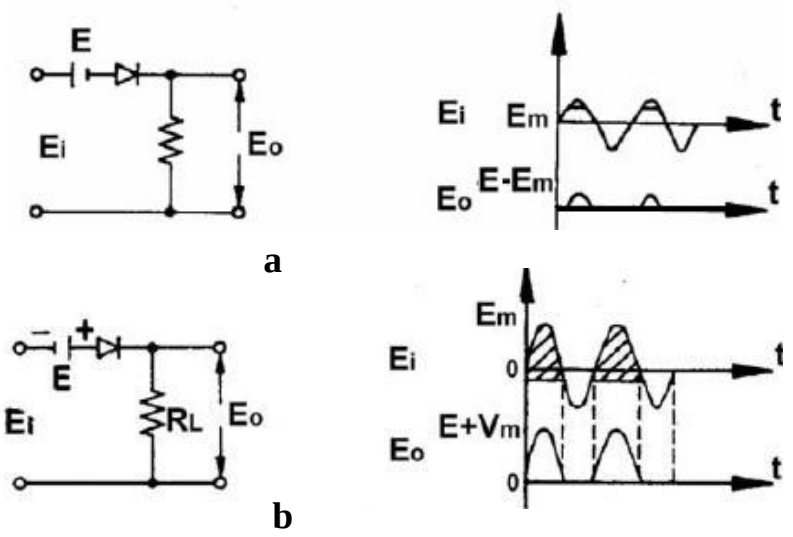


Fig. 2.14. Second type of Threshold Series Clipping Circuit

2.b). <u>Parallel Diode Clipping Circuit</u>

In this type of clippers, the diode is connected between output terminals. The on/off state of diode directly affects the output voltage (figs.2-15,16). These types of clippers may also have a non-zero threshold voltage by addition of a voltage series with diode. Following figures 2-15, 2-16 illustrate the clipping process.

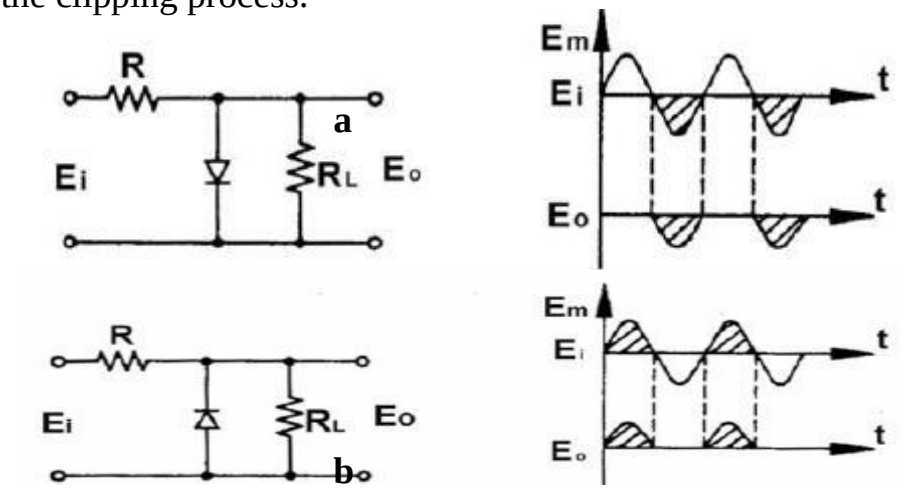


Fig. 2.15 . Zero Threshold Parallel Clippers

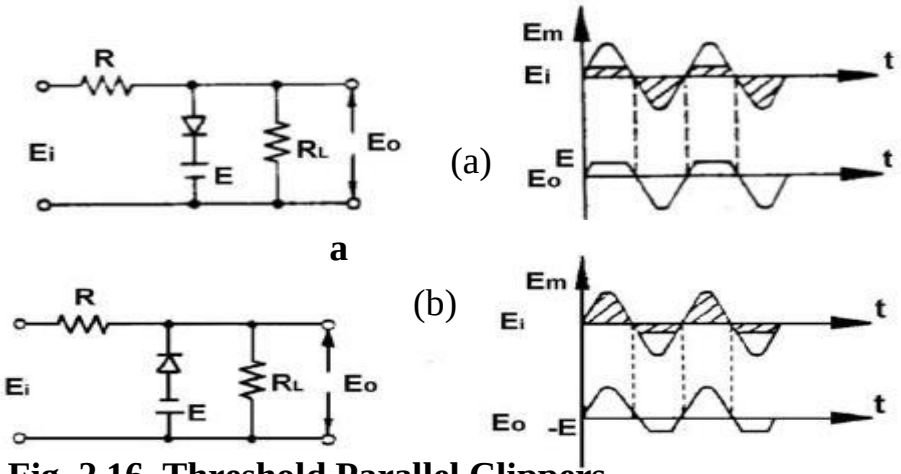


Fig. 2.16. Threshold Parallel Clippers

Summary

Biased Parallel *clipping* circuits

Comparison table of output voltage shapes

خلاصة لاشكال فولتية الخارج (V_o) لعدة احتمالات لربط كل من الدايود والبطارية :

هناك اربع احتمالات هي :

١. ان يربط الدايود بالاتجاه العلوي( ) والبطارية بالاتجاه العلوي كذلك ( ).

٢. ان يربط الدايود بالاتجاه العلوي ( ) والبطارية بالاتجاه السفلي كذلك ( ).

٣. ان يربط الدايود بالاتجاه السفلي ( ) والبطارية بالاتجاه العلوي كذلك ( ).

٤. ان يربط الدايود بالاتجاه السفلي ( ) والبطارية بالاتجاه السفلي كذلك ( ).

Input voltage		Battery direction اتجاه البطارية	
		البطارية للاعلى Up	البطارية للاسفل Down
Diode direction اتجاه الدايود	الدايود للاعلى Up	١ القص من الاعلى للجزء السفلي	٢ القص من الاسفل للجزء السفلي
	الدايود للاسفل Down	٣ القص من الاعلى للجزء العلوي	٤ القص من الاسفل للجزء العلوي

2-4 . Clamper Circuits and Voltage Doubler:

2-4-1. Clamper Circuits: or briefly clampers are used to change the D.C. level of a signal to a desired value.(**Fig 2.17**).

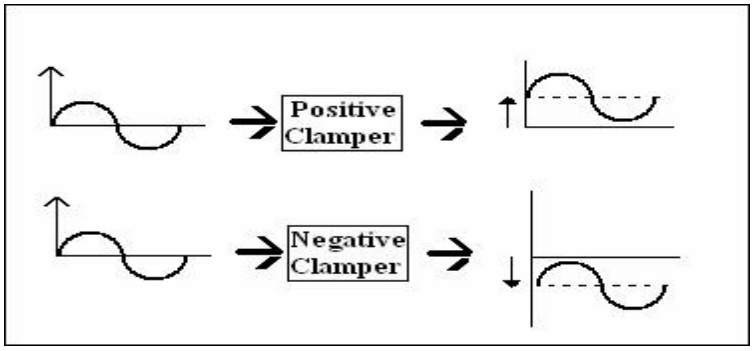


Fig 2.17. Inputs and outputs of positive and negative Clamper Circuits

Being different from clippers, clamping circuits uses a capacitor and a diode connection. When diode is in its **on** state, the output voltage equals to diode drop voltage (ideally zero) plus the voltage source, if any. Now let us examine the clamping process for the circuit in **Fig. 2.18.**

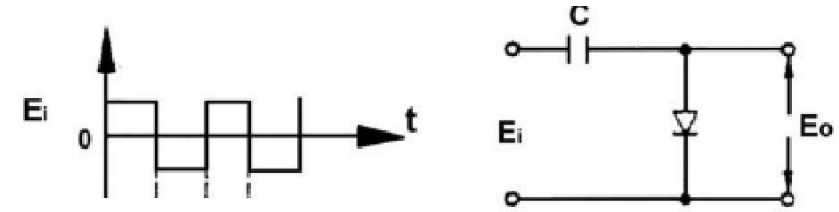


Fig 2.18. Typical Clamping Circuit

This circuit, in fact, is a series R-C circuit. The resistance of diode (several ohms above its drop voltage) and the small capacitance yield to a small time-constant for this circuit. This means that the capacitor will rapidly be charged if any input voltage, that is enough to switch on the diode, is applied. The diode will conduct during the positive cycle of the input signal (**Fig. 2.19-a**) and output voltage will be ideally zero (in practice this voltage equals ~0.6 V).

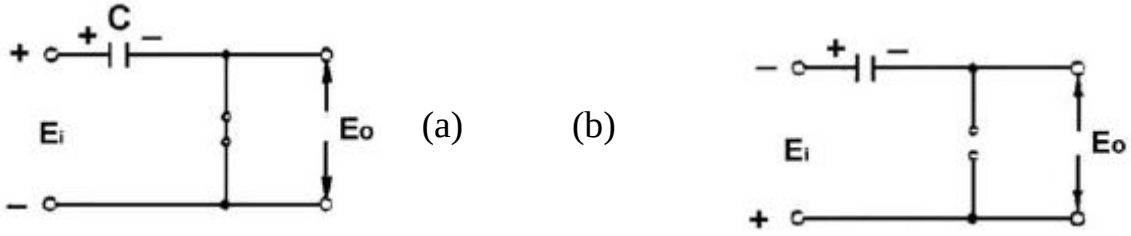


Fig 2.19. Diode conducts during (a)positive cycle and switched off(b) during negative cycle

Note that during positive cycle the capacitor is rapidly charged in inverse polarity with the input voltage. After transition to negative cycle, the diode becomes to its **off** state. In this case, the output voltage equals to the sum of the input voltage and the voltage across the terminals of the capacitor which have the same polarity with each other.(**Fig 2.19-b**).

$$E_0 = -\,(\,|Ei\,| + |Ec\,|\,)$$

The resulting signal after a complete cycle is shown below (fig.2-38).

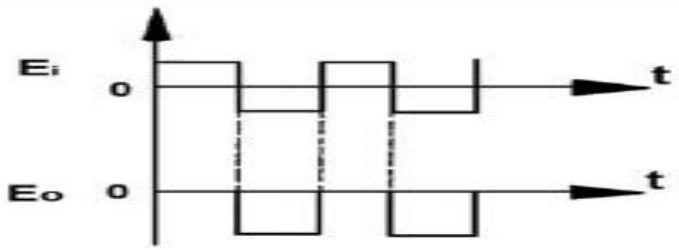


Fig. 2.20.Input and output waveforms of the Clamper

By this process, the input signal is shifted to negative D.C. value (its maximum value is ideally zero) without any change in its amplitude ideally.

There exist again modified versions of this circuit in which a threshold value is inserted for clamping. Following figures(fig 2-21 and fig.2-22) illustrate these modifications and resulting outputs.

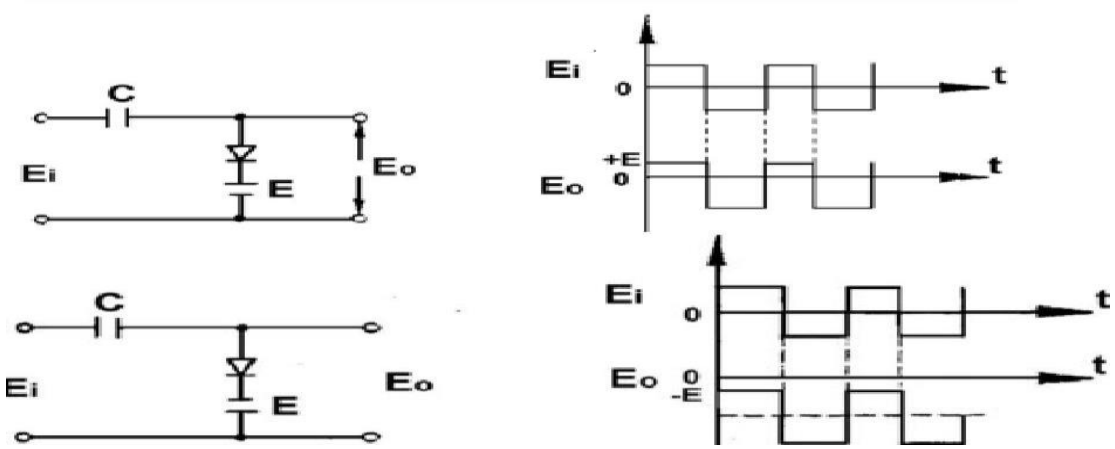


Fig.(2-21).one version of clamping circuits

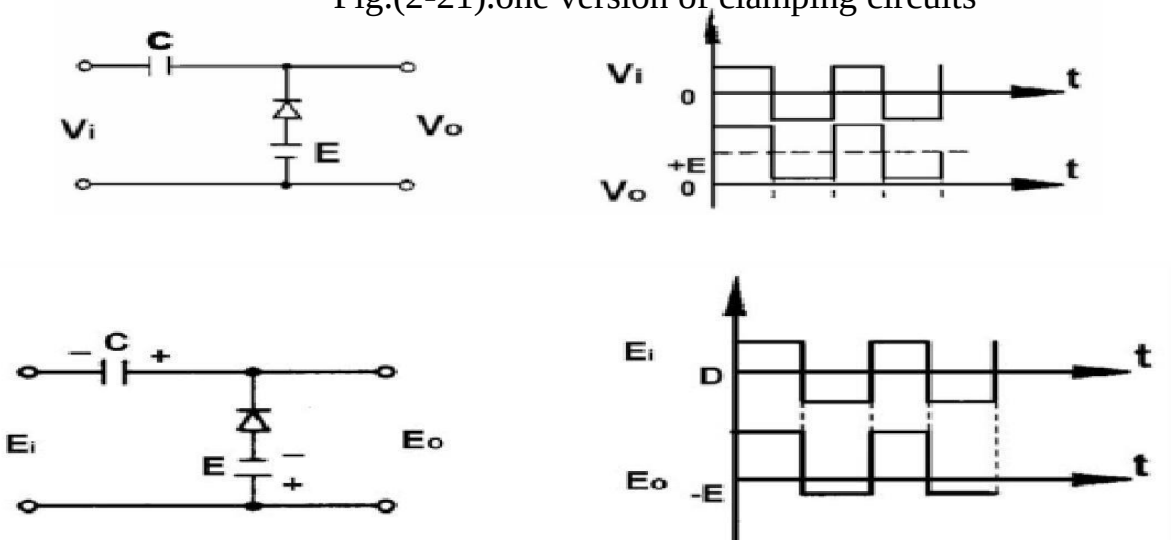


Fig. 2.22. Another version of clamping circuits

Summary

Biased Parallel *Clamping* circuits

Comparison table of output voltage shapes

خلاصة لاشكال فولتية الخارج (V_o) لعدة احتمالات لربط كل من الدايود والبطارية :

هناك اربع احتمالات هي :

١. ان يربط الدايود بالاتجاه العلوي( ) والبطارية بالاتجاه العلوي كذلك ( ).

٢. ان يربط الدايود بالاتجاه العلوي ( ) والبطارية بالاتجاه السفلي كذلك ( ).

٣. ان يربط الدايود بالاتجاه السفلي ( ) والبطارية بالاتجاه العلوي كذلك ( ).

٤. ان يربط الدايود بالاتجاه السفلي ( ) والبطارية بالاتجاه السفلي كذلك ( ).

		اتجاه البطارية Battery direction	
		البطارية للاعلى Up	البطارية للاسفل Down
اتجاه الدايود Diode direction	الدايود للاعلى Up	١ ترتفع الاشارة للاعلى ومستوى الاشارة فوق مستوى البطارية الموجب	٢ ترتفع الاشارة للاعلى ومستوى الاشارة فوق مستوى البطارية السالب
	الدايود للاسفل Down	٣ تنزل الاشارة للاسفل ومستوى الاشارة تحت مستوى البطارية الموجب	٤ تنزل الاشارة للاسفل ومستوى الاشارة تحت مستوى البطارية السالب

2-4-2. Voltage Doubler Circuits:

Another doubler circuit is the full-wave doubler of Fig. 2.23. During the positive half-cycle of transformer secondary voltage (see Fig. 2.24a) diode D1 conducts, charging capacitor C1 to a peak voltage V,,. Diode D2 is nonconducting at this time.
During the negative half-cycle (see Fig. 2.24b) diode D2 conducts, charging capacitor C2, while diode D1 is nonconducting. If no load current is drawn from the circuit, the voltage across capacitors C1 and C2 is 2V,, ,. If load current is drawn from the circuit, the voltage across capacitors C1 and C2 is the same as that across a capacitor fed by a full-wave rectifier circuit. One difference is that the effective capacitance is that of C1 and C2 in series, which is less than the capacitance of either C1 or C2 alone. The lower capacitor value will provide poorer filtering action than the single-capacitor filter circuit.

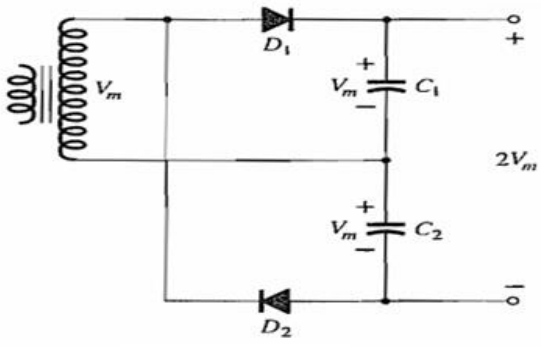


Fig. (2-23)

Full-wave voltage doubler.

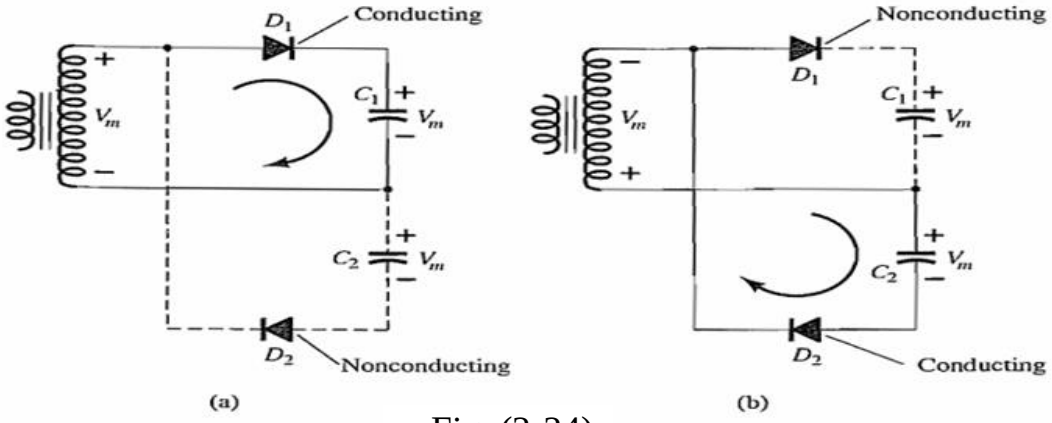


Fig. (2-24)

Alternate half-cycles of operation for full-wave voltage doubler.

The peak inverse voltage across each diode is 2V ,,, as it is for the filter capacitor circuit.
In summary, the half-wave or full-wave voltage-doubler circuits provide twice the peak voltage of the transformer secondary while requiring no center-tapped transformer and only 2Vm PIV (Peak Inverse Voltage) rating for the diodes.

Example : 2-20:

Determine the output waveform for the network of Fig. 2.74.

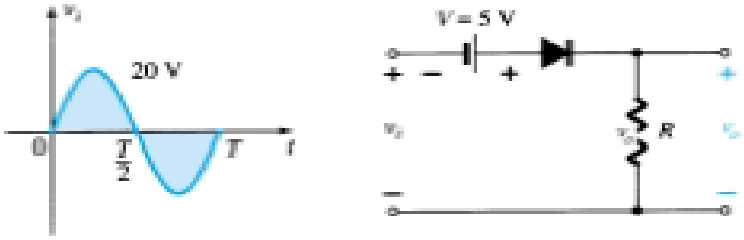


Figure 2.74 Series clipper for Example 2.20.

Solution

Past experience suggests that the diode will be in the "on" state for the positive region of v_i—especially when we note the aiding effect of $V = 5$ V. The network will then appear as shown in Fig. 2.75 and $v_o = v_i + 5$ V. Substituting $i_d = 0$ at $v_d = 0$ for the transition levels, we obtain the network of Fig. 2.76 and $v_i = -5$ V.

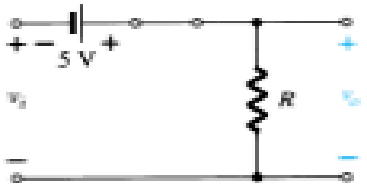
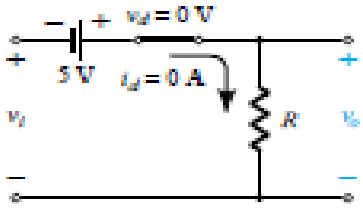


Figure 2.75 v_o with diode in the "on" state.



$v_o = v_R = i_R R = i_d R = (0)\,R = 0$ V

Figure 2.76 Determining the transition level for the clipper of Fig. 2.74.

For v_i more negative than -5 V the diode will enter its open-circuit state, while for voltages more positive than -5 V the diode is in the short-circuit state. The input and output voltages appear in Fig. 2.77.

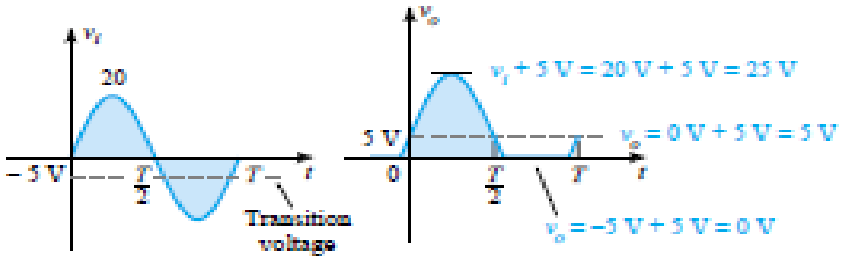


Figure 2.77 Sketching v_o for Example 2.20.

Repeat Example 2.20 for the square-wave input of Fig. 2.78.

EXAMPLE 2.21

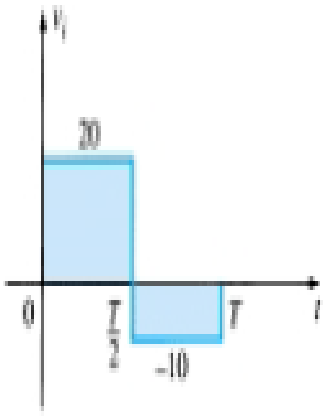


Figure 2.78 Applied signal for Example 2.21.

Solution

For $v_i = 20\text{ V}\ (0 \rightarrow T/2)$ the network of Fig. 2.79 will result. The diode is in the short-circuit state and $v_o = 20\text{ V} + 5\text{ V} = 25\text{ V}$. For $v_i = -10\text{ V}$ the network of Fig. 2.80 will result, placing the diode in the "off" state and $v_o = i_R R = (0)R = 0\text{ V}$. The resulting output voltage appears in Fig. 2.81.

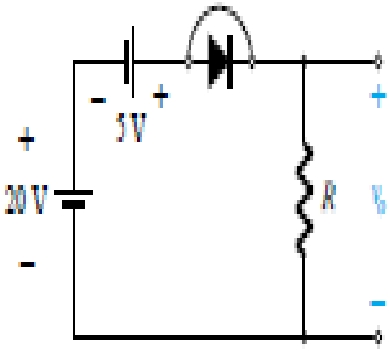


Figure 2.79 v_o at $v_i = +20$ V.

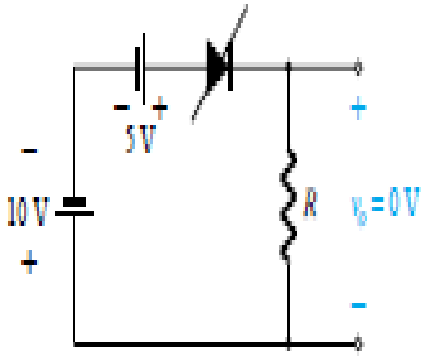


Figure 2.80 v_o at $v_i = -10$ V.

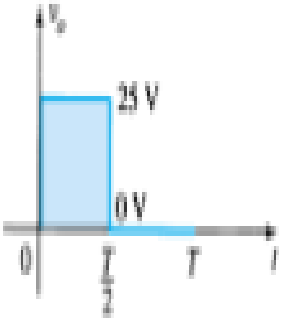


Figure 2.81 Sketching v_o for Example 2.21.

Note in Example 2.21 that the clipper not only clipped off 5 V from the total swing but raised the dc level of the signal by 5 V.

EXAMPLE 2.2

Determine v_o for the network of Fig. 2.83.

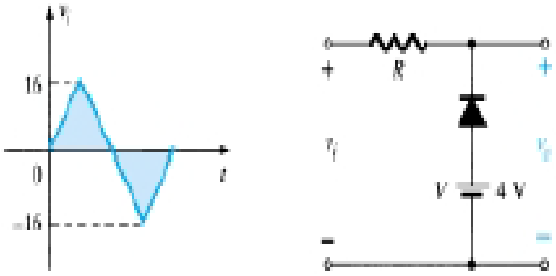


Figure 2.83 Example 2.22.

Solution

The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for the negative region of the input signal. For this region the network will appear as shown in Fig. 2.84, where the defined terminals for v_o require that $v_o = V = 4$ V.

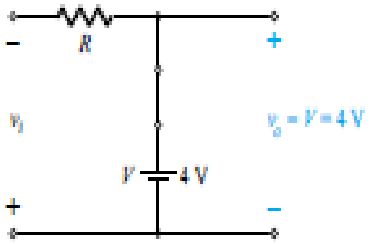


Figure 2.84 v_o for the negative region of v_i.

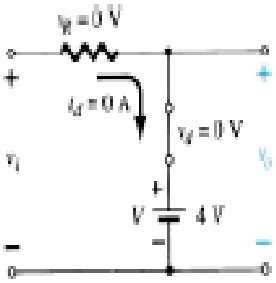


Figure 2.85 Determining the transition level for Example 2.22.

The transition state can be determined from Fig. 2.85, where the condition $i_d = 0$ A at $v_d = 0$ V has been imposed. The result is v_i (transition) $= V = 4$ V.

Since the dc supply is obviously "pressuring" the diode to stay in the short-circuit state, the input voltage must be greater than 4 V for the diode to be in the "off" state. Any input voltage less than 4 V will result in a short-circuited diode.

For the open-circuit state the network will appear as shown in Fig. 2.86, where $v_o = v_i$. Completing the sketch of v_o results in the waveform of Fig. 2.87.

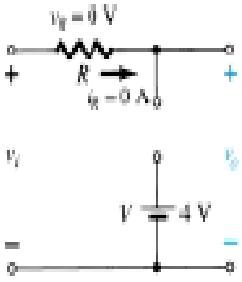


Figure 2.86 Determining v_o for the open state of the diode.

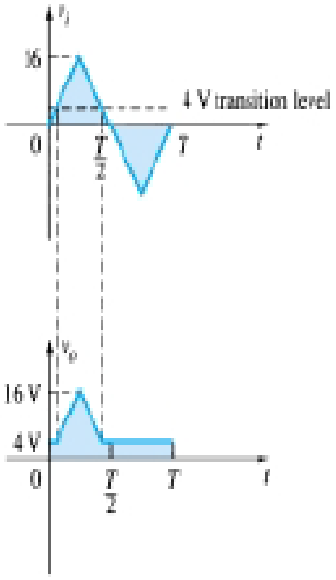


Figure 2.87 Sketching v_o for Example 2.22.

Repeat Example 2.22 using a silicon diode with $V_T = 0.7$ V. EXAMPLE 2.23

Solution

The transition voltage can first be determined by applying the condition $i_d = 0$ A at $v_d = V_D = 0.7$ V and obtaining the network of Fig. 2.88. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_T - V = 0$$

and

$$v_i = V - V_T = 4\text{ V} - 0.7\text{ V} = 3.3\text{ V}$$

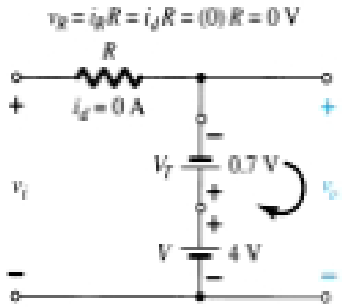


Figure 2.88 Determining the transition level for the network of Fig. 2.83.

For input voltages greater than 3.3 V, the diode will be an open circuit and $v_o = v_i$. For input voltages of less than 3.3 V, the diode will be in the "on" state and the network of Fig. 2.89 results, where

$$v_o = 4\text{ V} - 0.7\text{ V} = 3.3\text{ V}$$

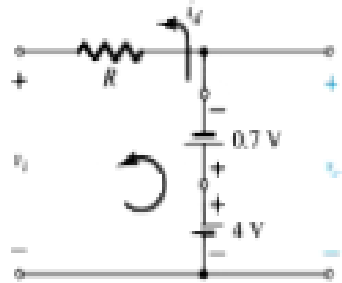


Figure 2.89 Determining v_o for the diode of Fig. 2.83 in the "on" state.

The resulting output waveform appears in Fig. 2.90. Note that the only effect of V_T was to drop the transition level to 3.3 from 4 V.

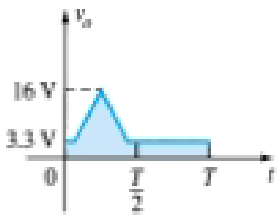


Figure 2.90 Sketching v_o for Example 2.23.

There is no question that including the effects of V_T will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of V_T, will not be that difficult.

Summary of Clipping Circuits

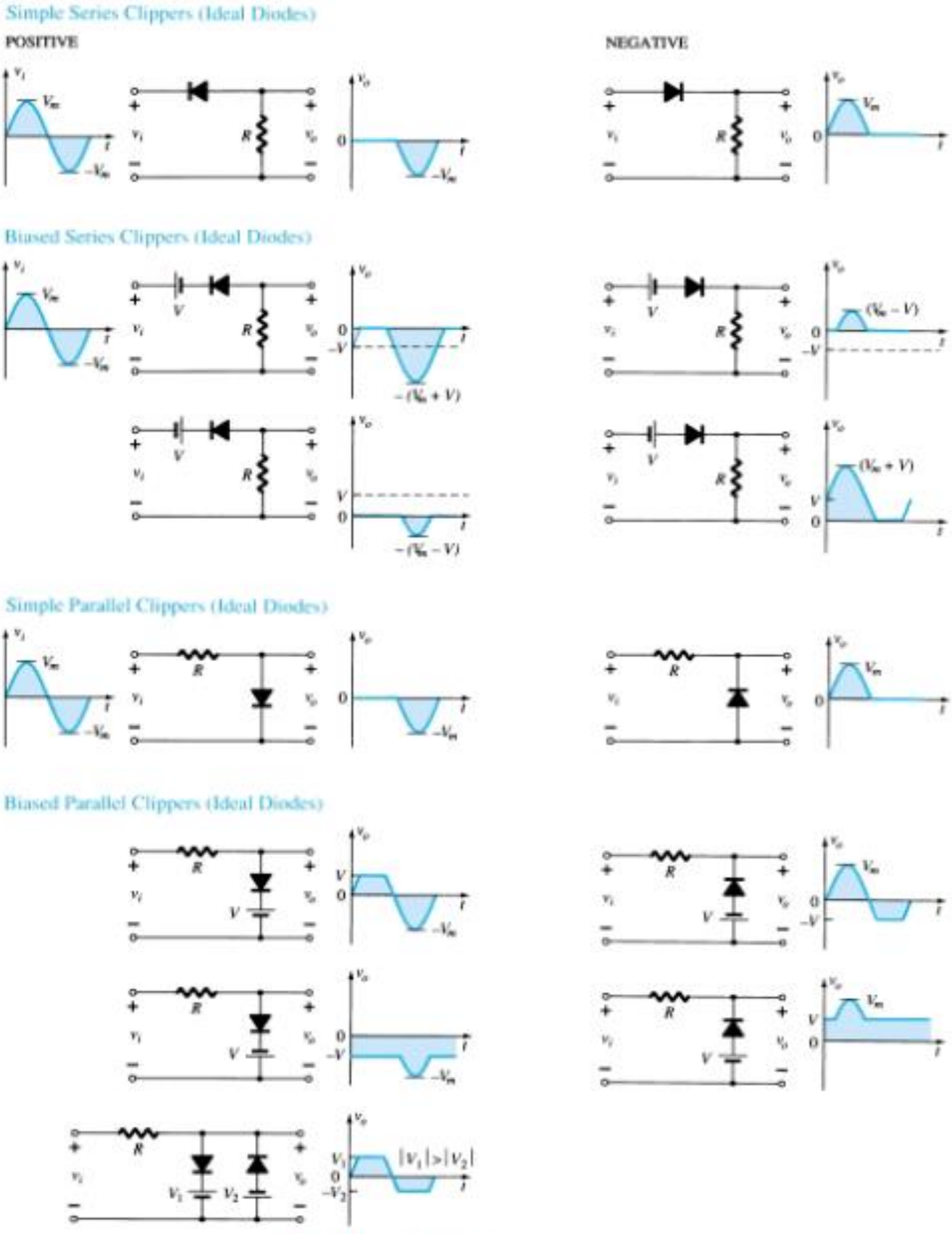


Figure 2.91 Clipping circuits.

Some Examples from Boylestad Book

Examples on Clamping circuits:

EXAMPLE 2.24 Determine v_o for the network of Fig. 2.96 for the input indicated.

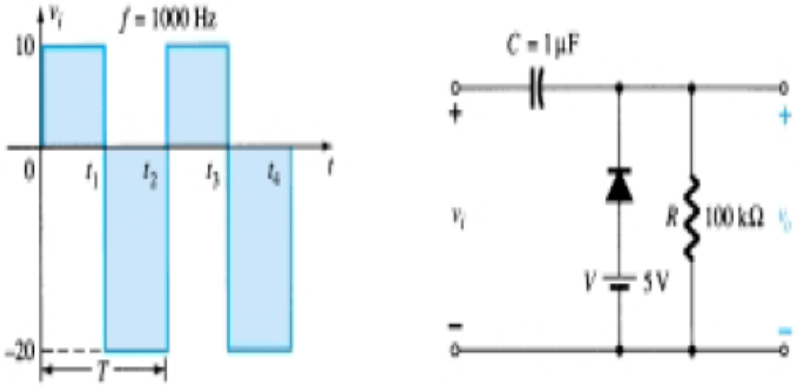


Figure 2.96 Applied signal and network for Example 2.24.

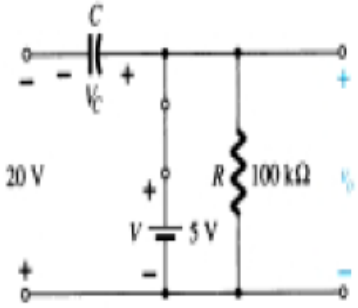


Figure 2.97 Determining v_o and V_C with the diode in the "on" state.

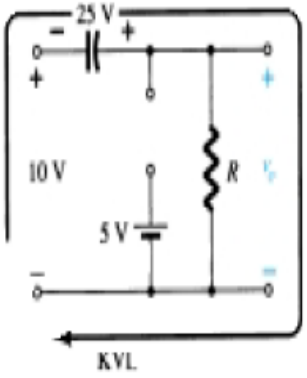


Figure 2.98 Determining v_o with the diode in the "off" state.

Solution

Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state as recommended by comment 1. For this interval the network will appear as shown in Fig. 2.97. The output is across R, but it is also directly across the 5-V battery if you follow the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5$ V for this interval. Applying Kirchhoff's voltage law around the input loop will result in

$$-20\text{ V} + V_C - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V}$$

The capacitor will therefore charge up to 25 V, as stated in comment 2. In this case the resistor R is not shorted out by the diode but a Thévenin equivalent circuit of that portion of the network which includes the battery and the resistor will result in $R_{Th} = 0\ \Omega$ with $E_{Th} = V = 5$ V. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.98.

The open-circuit equivalent for the diode will remove the 5-V battery from having any effect on v_o, and applying Kirchhoff's voltage law around the outside loop of the network will result in

$$+10\text{ V} + 25\text{ V} - v_o = 0$$

and

$$v_o = 35\text{ V}$$

The time constant of the discharging network of Fig. 2.98 is determined by the product RC and has the magnitude

$$\tau = RC = (100\ \text{k}\Omega)(0.1\ \mu\text{F}) = 0.01\ \text{s} = 10\ \text{ms}$$

The total discharge time is therefore $5\tau = 5(10\ \text{ms}) = 50\ \text{ms}$.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.99 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

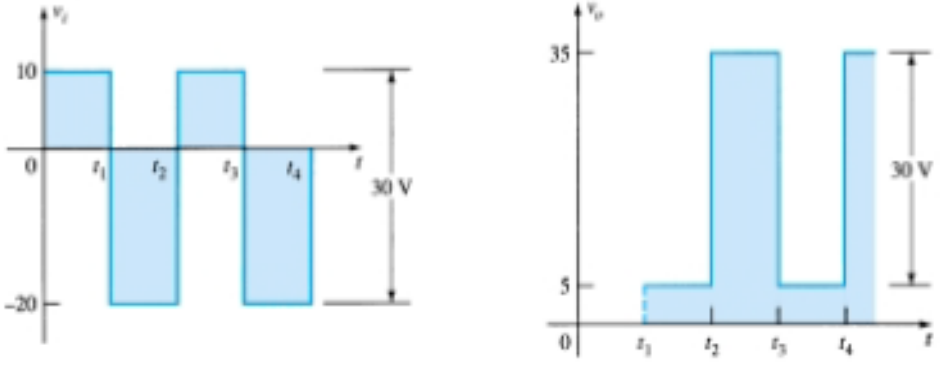


Figure 2.99 v_i and v_o for the clamper of Fig. 2.96.

EXAMPLE 2.25

Repeat Example 2.24 using a silicon diode with $V_T = 0.7$ V.

Solution

For the short-circuit state the network now takes on the appearance of Fig. 2.100 and v_o can be determined by Kirchhoff's voltage law in the output section.

$$+5\ \text{V} - 0.7\ \text{V} - v_o = 0$$

and

$$v_o = 5\ \text{V} - 0.7\ \text{V} = 4.3\ \text{V}$$

For the input section Kirchhoff's voltage law will result in

$$-20\ \text{V} + V_C + 0.7\ \text{V} - 5\ \text{V} = 0$$

and

$$V_C = 25\ \text{V} - 0.7\ \text{V} = 24.3\ \text{V}$$

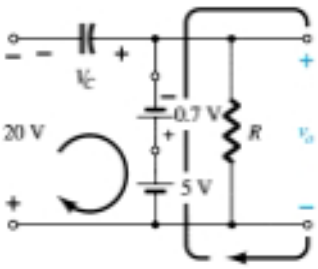


Figure 2.100 Determining v_o and V_C with the diode in the "on" state.

For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.101, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10\ \text{V} + 24.3\ \text{V} - v_o = 0$$

and

$$v_o = 34.3\ \text{V}$$

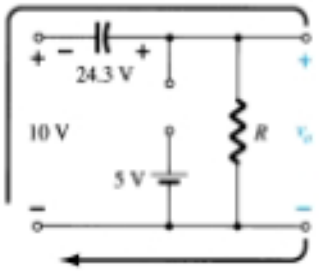


Figure 2.101 Determining v_o with the diode in the open state.

The resulting output appears in Fig. 2.102, verifying the statement that the input and output swings are the same.

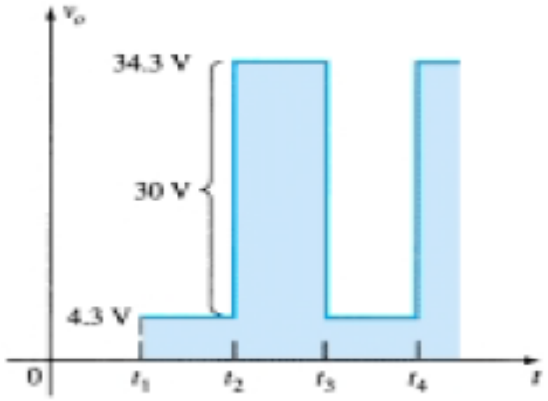


Figure 2.102 Sketching v_o for the clamper of Fig. 2.96 with a silicon diode.

Summary of Clamping circuits:

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.103. Although all the waveforms appearing in Fig. 2.103 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.104 for a network appearing in the bottom right of Fig. 2.103.

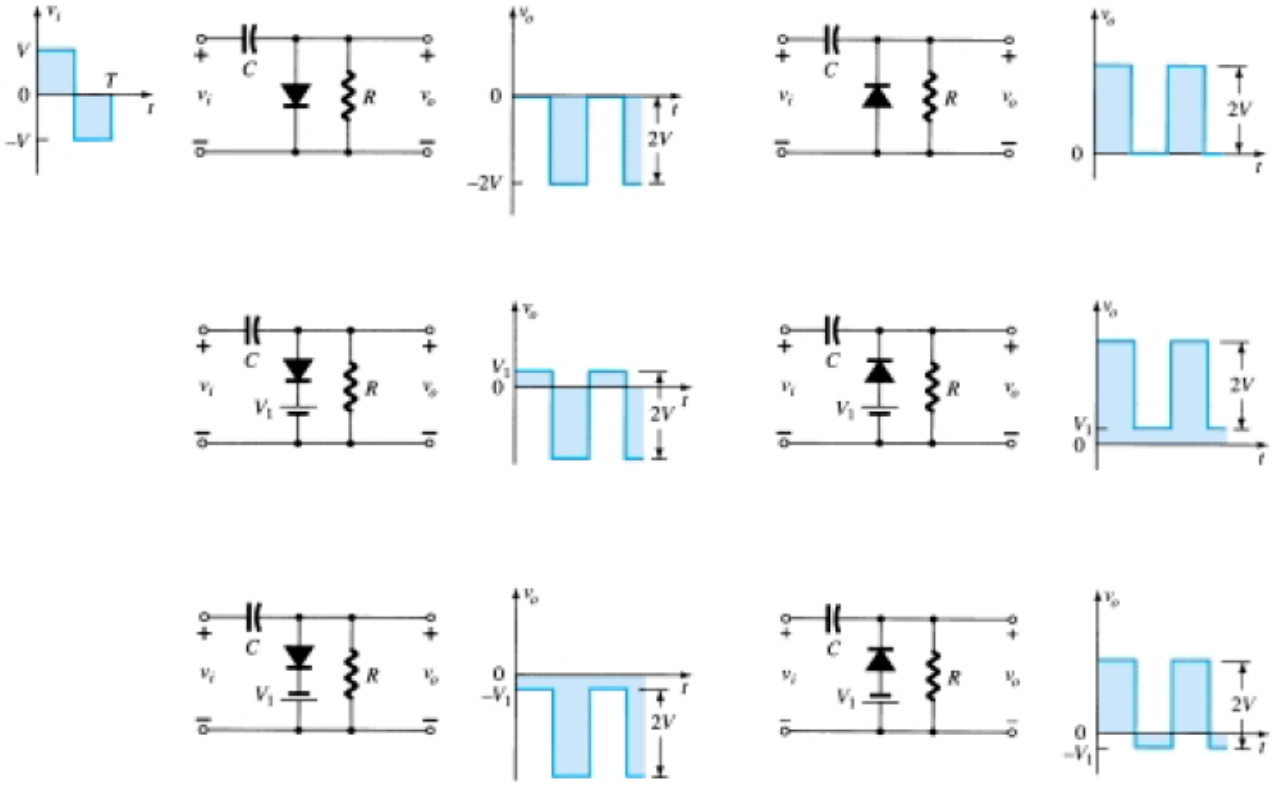


Figure 2.103 Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

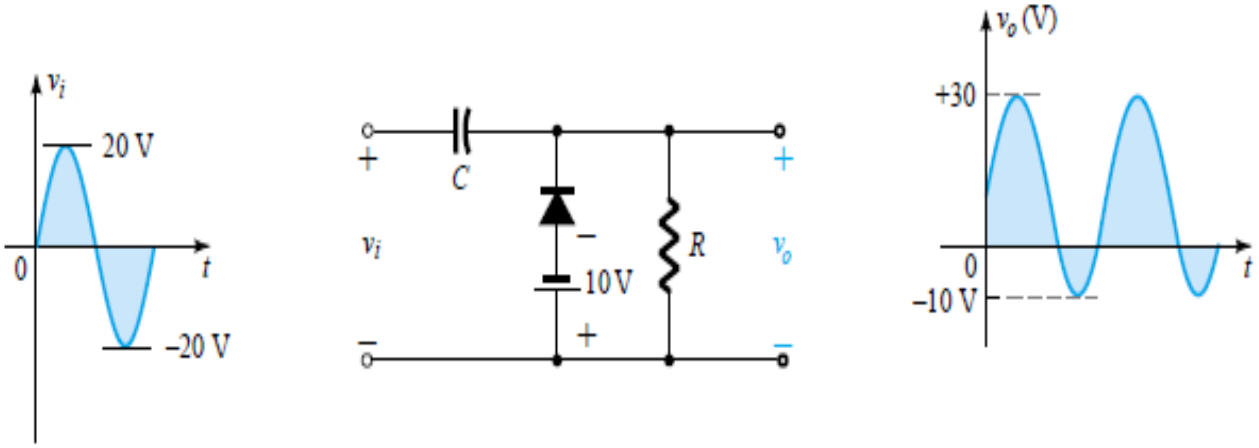


Figure 2.104 Clamping network with a sinusoidal input.

Review Questions:

Please see the relevant problems in :
" Electronic Devices and Circuit Theory ", By: Boylestad, R. and Nashelsky, L., 7th edition , Chapter -2 , page 103-111 .
(The Electronic version of this book is available at Internet and at the department- for anyone who want it).