❖ Full – Wave rectification

The dc level obtained from a sinusoidal input by half wave rectifier can be improved 100% using a process called Full Wave Rectification four diodes in a bridge configuration can be used full wave rectifier as shown in Fig. 2.1.

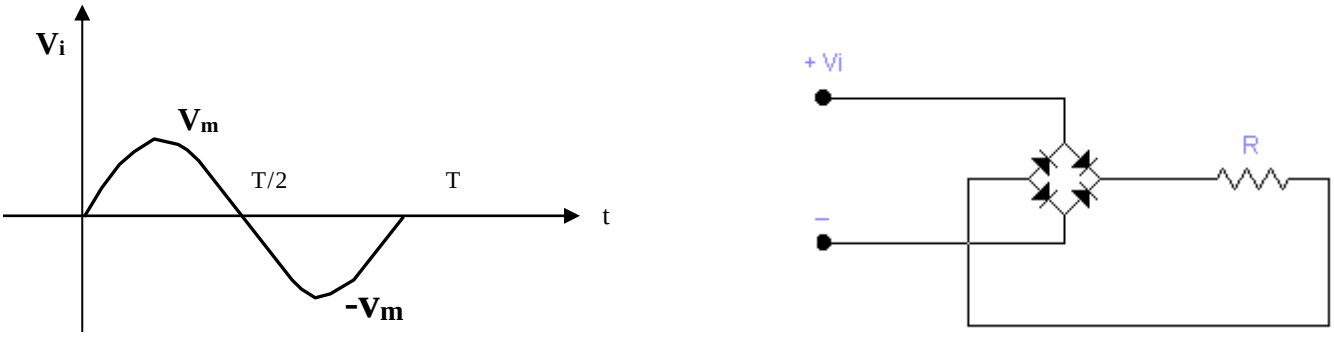


Fig. 2.1

- For the positive region of the input the conducting diodes are D_2 and D_3 while D_1 and D_4 are in the off state.
- For the negative region of the input the conducting diode are D_1 and D_4 while D_2 and D_3 are in the off state.
- The dc level for full wave rectifier is twice that optioned for for a half wave system
  $\therefore$ average (dc) level = 0.636 V_m
  and over one full cycle the input and output voltage is shown in Fig. 2.2.

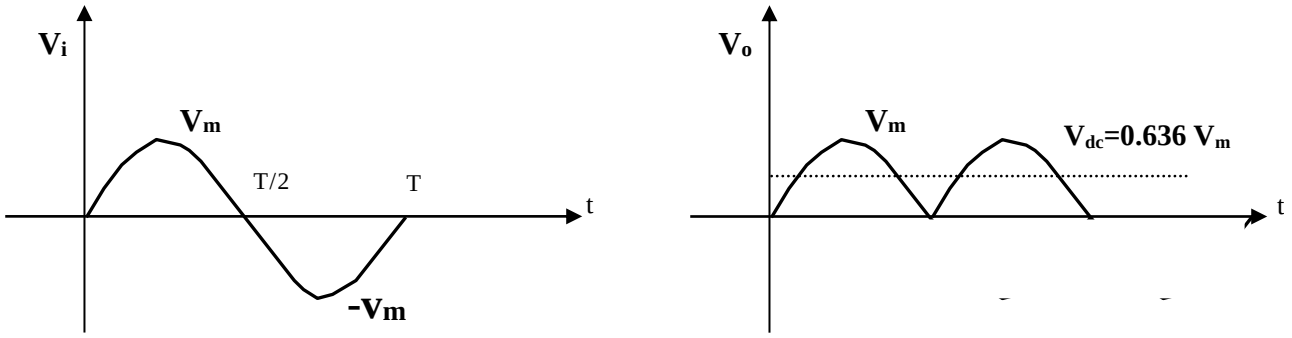


Fig. 2.2

The effect of V_0 has also doubled as shown in Fig. 2.3 for silicon diode during the conduction state (for positive region)

$\therefore V_{dc} = o.636Vm \Big|_{V_m >> 2V_T}$ and if V_m is close to $2V_T$ $\therefore V_{dc} = o.636\ (V_m - 2V_T)$

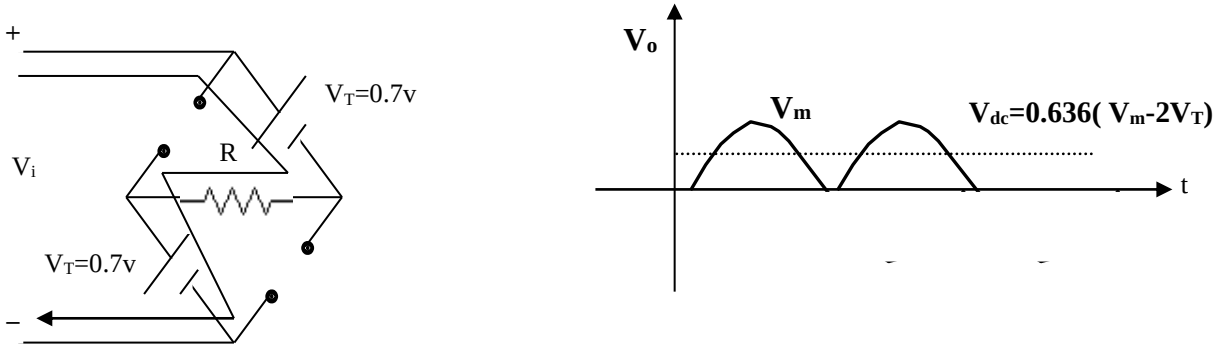


Fig. 2.3

A second popular full wave rectifier used only two diodes but requiring a center tapped (CT) to establish the input signal across each section of the secondary of the transformer as shown in Fig. 2.4.

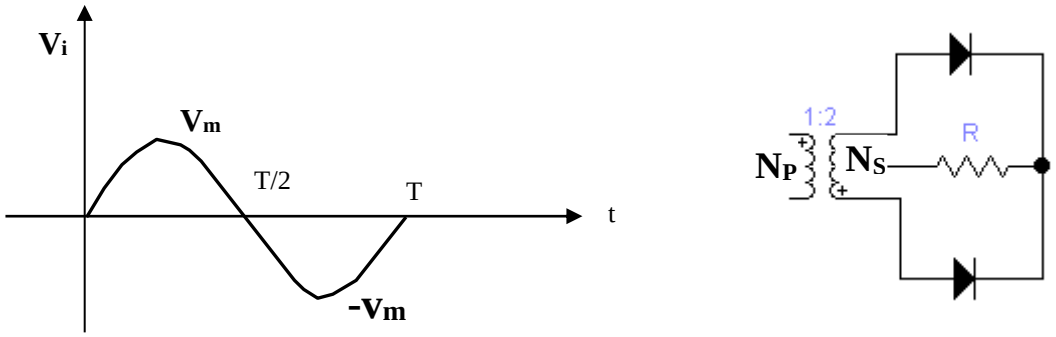
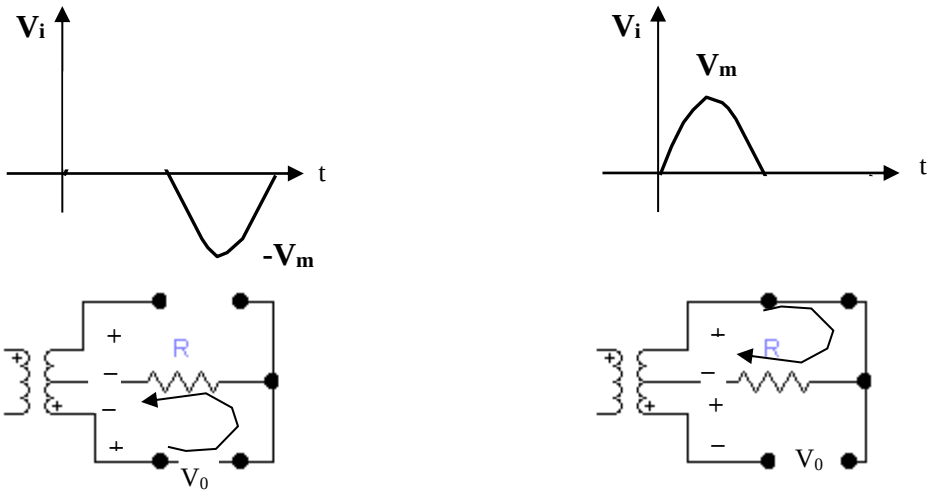


Fig. 2.4

$N_P/N_S=V_P/V_S$

- During the positive portion of V_i applied to the transformer the diode D_1 is short circuit and the diode D_2 is open circuit.
- During the negative portion of V_i applied to the transformer, the diode D_1 is open circuit and the diode D_2 is short circuit as shown in Figure.



For -ve region **For +ve region**

PIV (peak inverse voltage) for each diode for this full wave rectifier can be determined from Fig. 2.5.

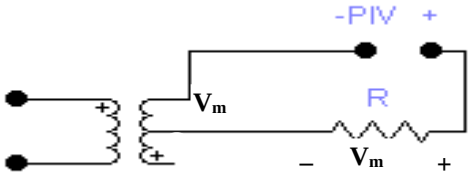


Fig. 2.5

Inserting the maximum voltage for the secondary voltage then
PIV = $V_{Secondary} + V_R$
PIV = $V_m + V_m = 2V_m$ (For transformer full wave rectification)

Example:
Determine the output waveform for the network of Fig. 2.6 and calculate the output dc level and the required PIV of each diode.

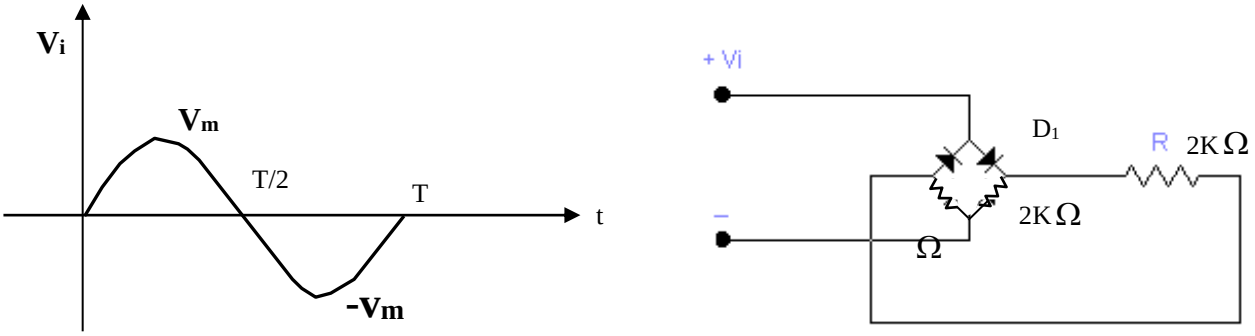


Fig. 2.6

Solution:
The network will appear as shown in Fig. 2.7 for +ve region of the input voltage. D_1 is on, D_2 is off

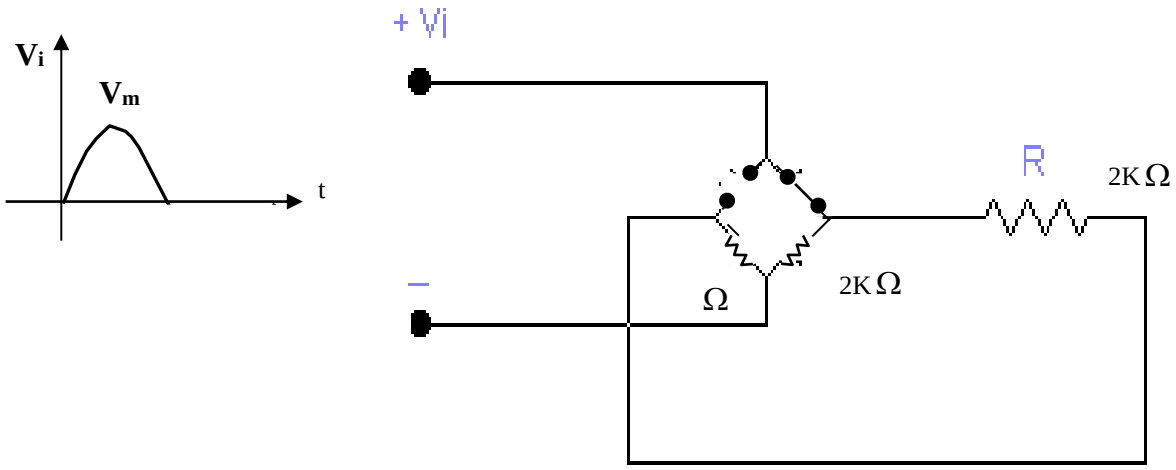
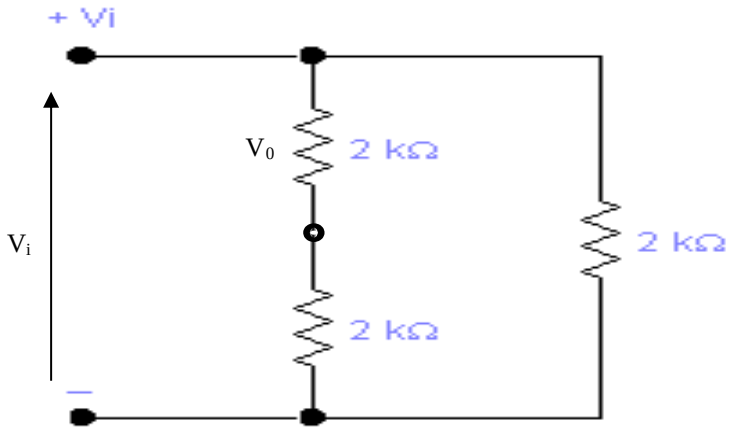


Fig. 2.7

Redrawing the network will result in the configuration of Fig. 2.8
Were $V_0 = (1/2)V_i$

V_0 max = $(1/2)V_i$ max = (1/2)(10) = 5V

During the negative, reversing the roles of diodes (D_1 is off and D_2 is on).



The effect of removing two diodes from the bridge configuration was therefore to reduce the available dc level to the following

$\mathbf{V_{dc} = 0.636(5) = 3.18\ V}$

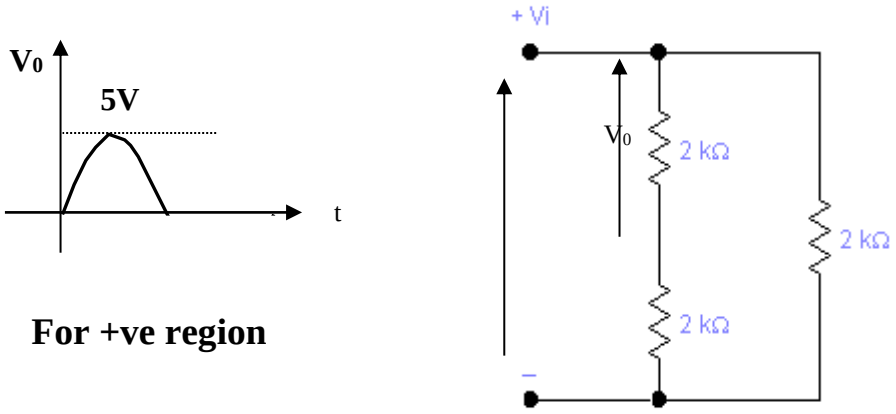


Fig. 2.8

V_0 is shown in Fig. 2.9.

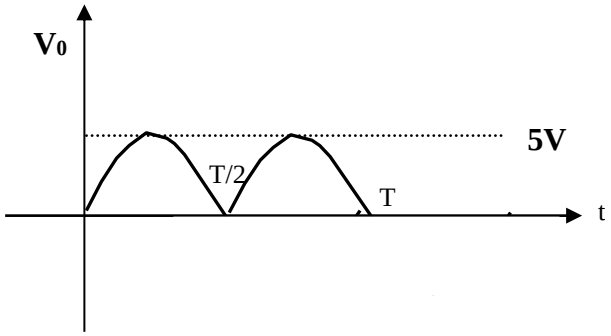


Fig. 2.9

The **PIV** is equal to the maximum voltage across R, which is (**5V**).

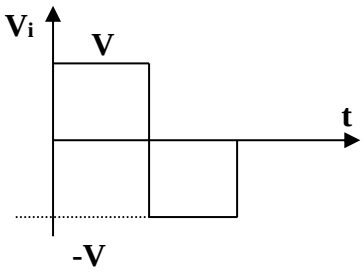
❖ Clippers

There are a variety of diode networks called clippers that have the ability to clip off a portion of the input signal without distorting the remaining part. The half wave rectifier is an example of the simplest form of diode clipper. There are two categories of clippers: -

Series clipper: the diode is in the series with load.
Parallel clipper: the diode is in the parallel to the load.

➢ Series clipper

The response of the series clipper of Fig. 2.10 to a different wave from is shown in Figs. 2.11a and 2.11b.



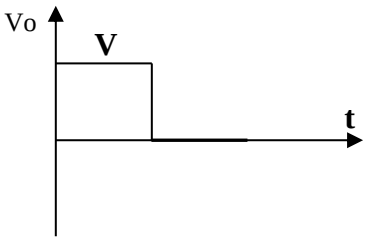


Fig. 2.11a

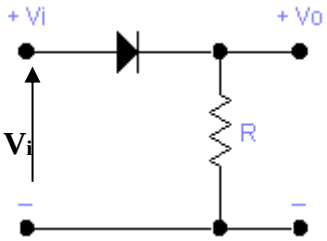
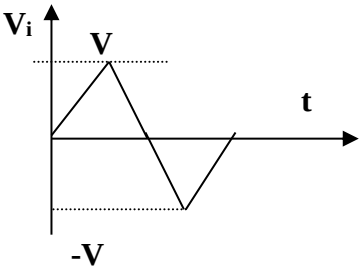


Fig. 2.10



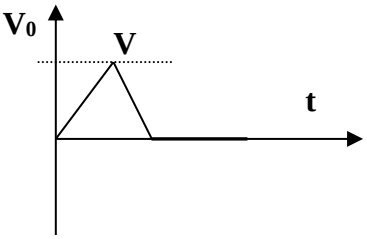


Fig. 2.11b

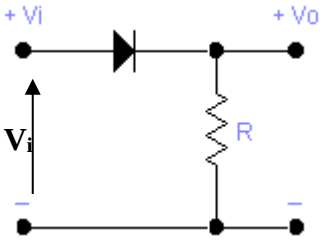
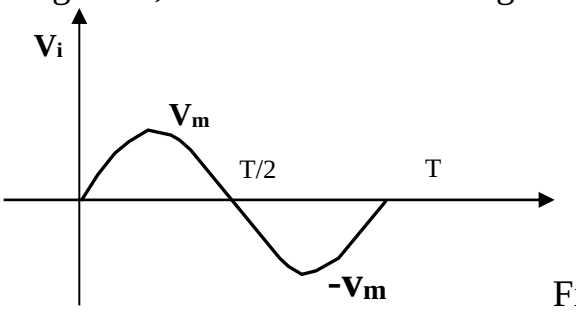


Fig. 2.10

The addition of a dc supply such as shown in Fig. 2.11 can have a clear effect on the output of a clipper. There is no general procedure for analyzing network such as shown in Fig. 2.11, but there are few thoughts to keep in mind during the solution of problem.



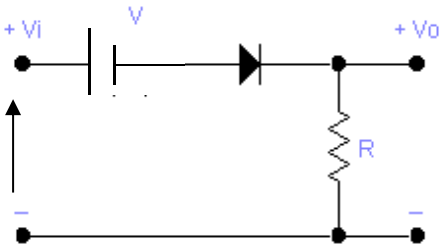


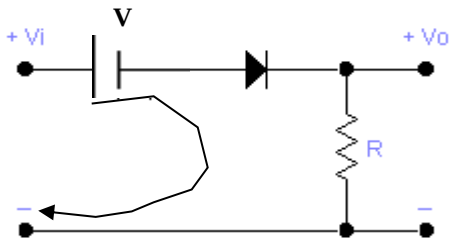
Fig. 2.11

1. Determine the diode is an open or short circuit (off or on state).
2. Determine the applied voltage that will cause a change in state for the diode (transition voltage).

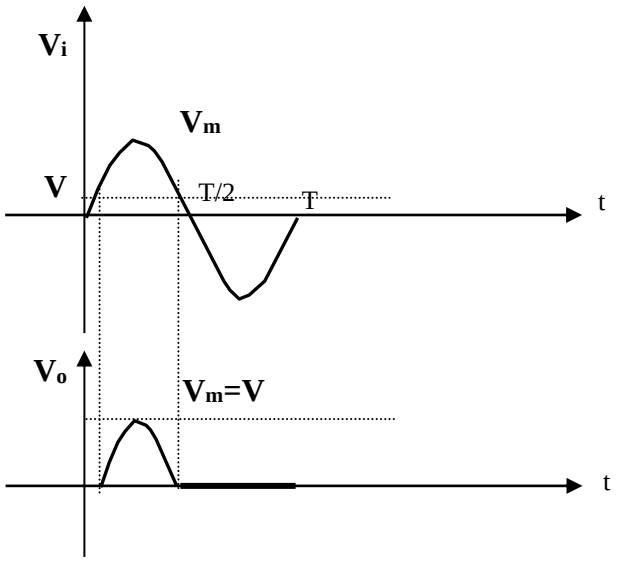
$$V_i > V_{dc}$$

3. Defined terminals and polarity of V_0 when the diode is in the short circuit state, the output voltage V_0 can be determined by using kirchoffs law

$$V_i - V - V_0 = 0$$
$$\therefore V_0 = V_i - V$$



4. Sketch the input signal above the transition output and determine the output at instantaneous values of the input by using the above formula (for each case)



Example:
Determine the output waveform for the network of Fig. 2.12?

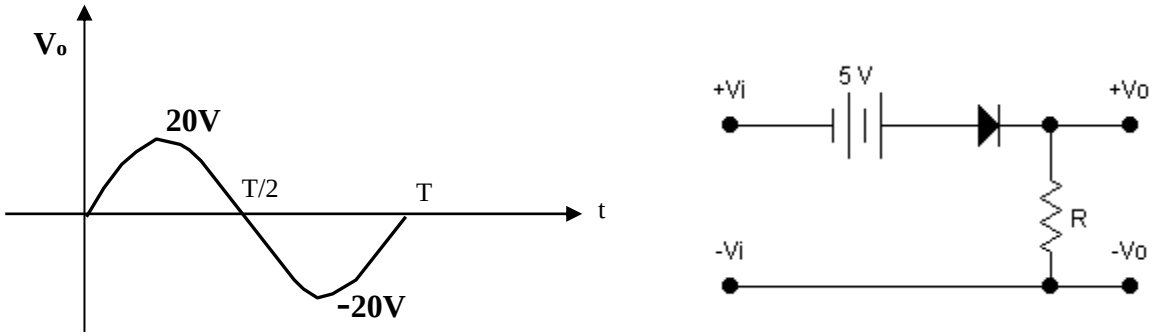


Fig. 2.12

Solution:
The diode in the state on for the positive region of V_i (and effect of V=5v aid this state).

The network will then appear as shown in Fig. 2.13

$\mathbf{V_0 = V_i + 5}$

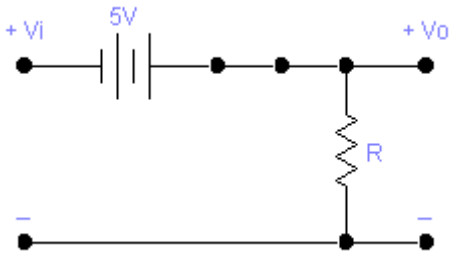


Fig. 2.13

For transition voltage substituting $i_d = 0$ at $V_d = 0 \rightarrow V_0 = 0$

$\therefore 0 = V_i + 5$

$\therefore V_i = -5V$

For voltages more the -5V the diode is in the short circuit.

For voltages less the –5V the diode is in the open circuit

The input and output voltages shown in Fig. 2.14 by using the equation

$V_0 = V_i + 5$

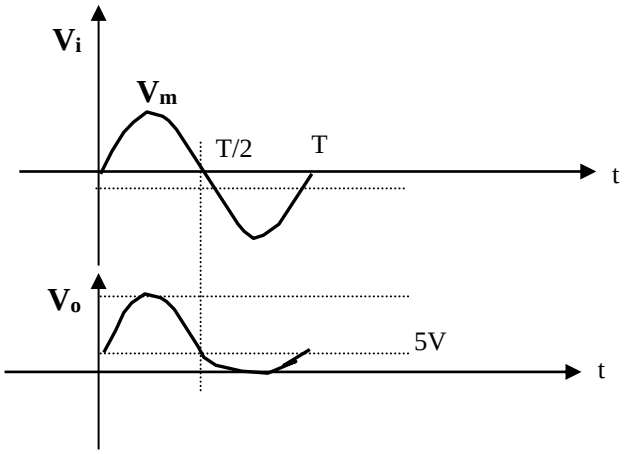
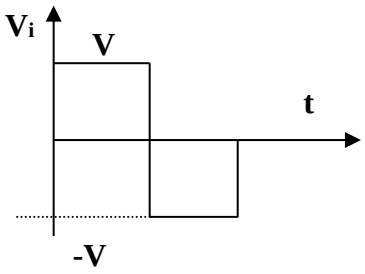
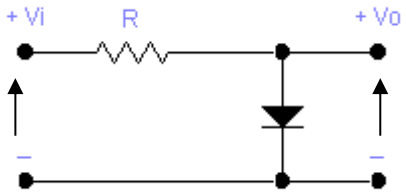


Fig. 2.14

➢ **Parallel Clipper**

The diode is in the parallel of to the load. The analysis of parallel configuration is very similar to that applied to series configuration.





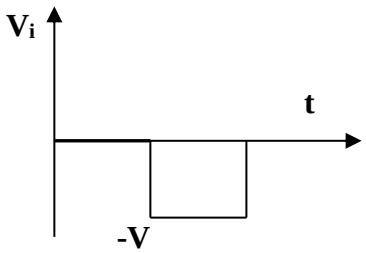


Fig. 2.15

Example:
Determine V_0 for the network of Fig. 2.16

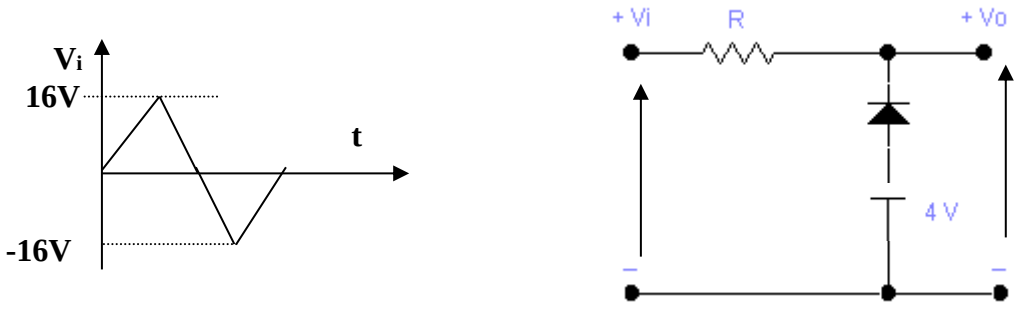


Fig. 2.16

Solution:
The diode will be in the on state for negative region of the input signal. For this region of the input the network will appear as shown in Fig. 2.17, V_o =4V

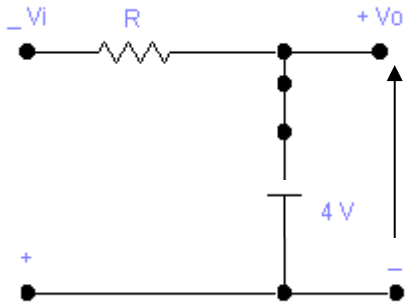


Fig. 2.17

The transition state can be determined, whose id =0A at V_d =o

$\therefore V_i$ (transition) = 4V

The diode will be in state off for input voltage greater then 4V and $V_o = V_i$ as shown in Fig. 2.18

The input and output voltage shown in Fig. 2.19

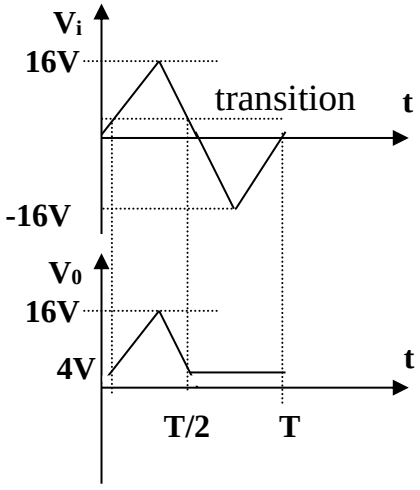


Fig. 2.19

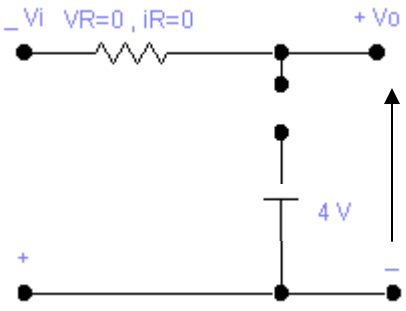


Fig. 2.18

❖ **Clampers**

The clamping network will clamp a signal to a different dc level. The network must have a capacitor, a diode, and a resistive element but it can also employ an in depend dc supply to introduce an addition shift.

The magnitude of R and C must be chosen such that the time constant τ=RC is large enough to ensure that the voltage across the capacitor does not discharge during off state of the diode.

We will assume that the capacitor will fully charge or discharge in five-time constant (τ). The network of Fig. 2.20 will clamp the input signal to zero level for ideal diode.

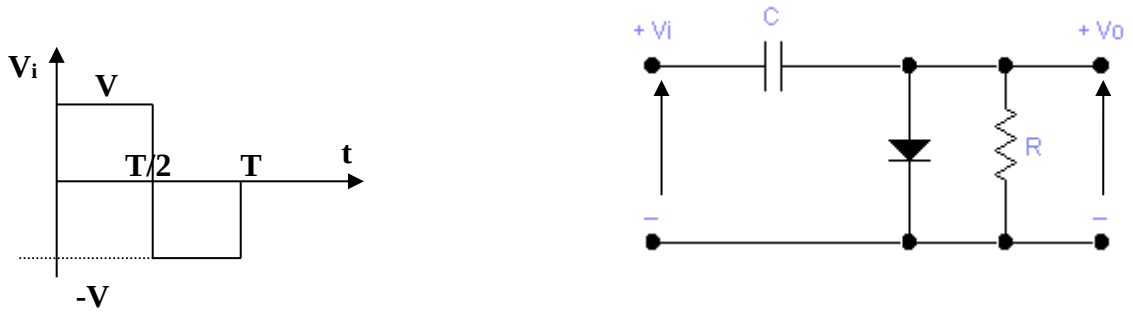


Fig. 2.20

- During the interval o → T\2 the network as shown in Fig. 2.21 the diode is in short cct (on state) shorting out the effect of the resistor R. Thus, the capacitor will charge to V very quickly and $V_o = 0$.

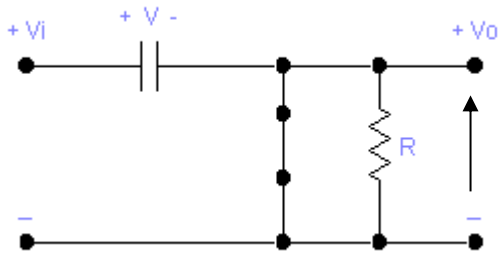


Fig. 2.21

- During the interval (T\2 → T) the network as shown in Fig. 2.22, the diode is in open cct off state. Now R is back in the network, the time constant determined by the RC is large to establish a discharge period (5τ) mush greater than (T\2 → T), and it can be assumed that the capacitor holds the charge and therefore voltage (V=Q/C). Thus, by using kirchoff's voltage law

$-V-V-V_o = 0$

$\therefore V_o = -2V$

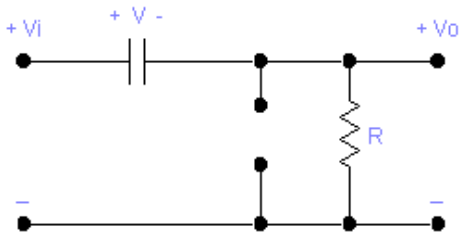


Fig. 2.22

The output signal is clamped to 0V for the interval 0 to T\2 but maintains the same total swing (2V) as shown in Fig. 2.23.

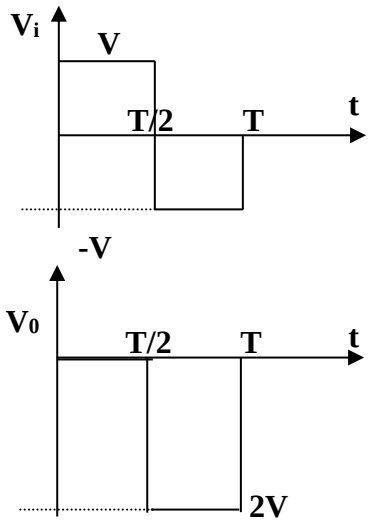


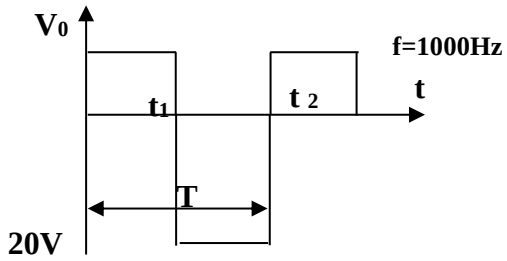
Fig. 2.23

- For clamping networks, the total swing of the output is equal to the total swing of the input signal. The following steps may be used for analyzing clamping network:-

1. State the analysis of clamping networks by considering that part of the input signal will forward bias the diode.
2. During the period that diode in on state as swing the capacitor will charge up instantaneously to level determined by the voltage across the capacitor in its equivalent open circuit state.
3. Assume during the period the diode is an open cct (off state) the capacitor will hold on the charge voltage.
4. Applying Kirchoff's law to determine V_o for both state on and off.
5. The general rule that the swing of the output voltage is equal to the total.

Example

Determine V_o for the network of Fig. 2.24?



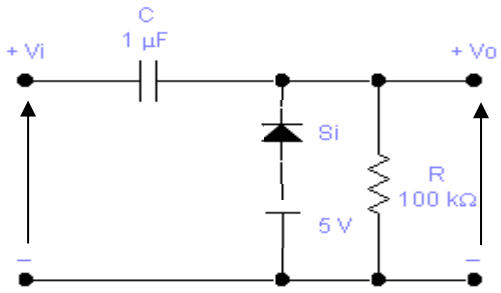


Fig. 2.24

Solution:

F = 1000Hz $\therefore$ T =1 msec

t2 - t1 = T/2 =0.5 msec

For the short circuit state, the network will appear as shown in Fig. 2.25 and V_o can be determined by kirchoff's voltage V_o in the output section

+5 – 0.7 – V_o =0

$\therefore V_o$ =4.3 V

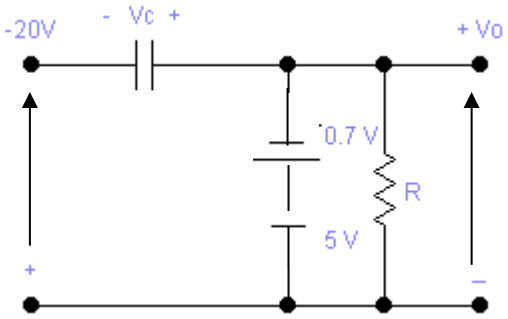


Fig. 2.25

For input section kirchoff's voltage law

-20V + V_c + 0.7 – 5 =0

$\therefore V_c$ =24.3 V (thus the capacitor will charge up to 24.3V)

For the period t2→t3 the diode in open cct state, the network will appear as shown in Fig. 2.26. Applying Kirchoffs voltage law around the outside loop to find V_o

10V + 24.3 – V_o =0,

$\therefore V_o$ = 34.3V

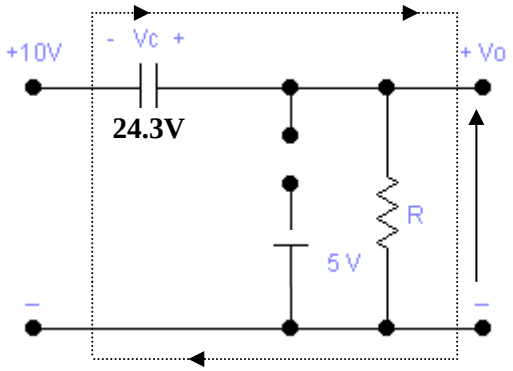


Fig. 2.26

- The resulting output in Fig. 2.27 note that the total swing of 30V matches the input signal swing as noted in step 5.

- The time constant of the network τ can be determined by the product RC and has the magnitude.

τ= RC = (100KΩ)(1μF) =0.01s = 10ms

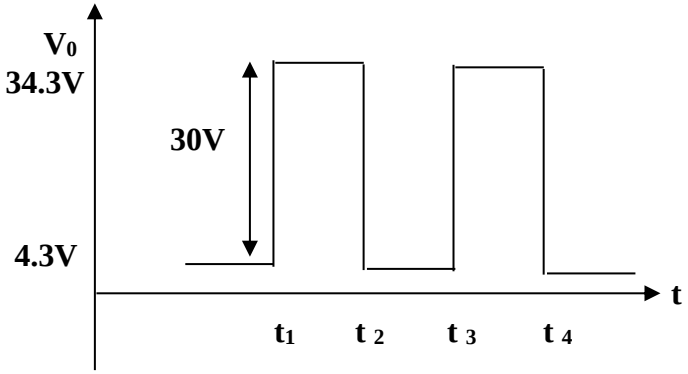


Fig. 2.27

The total discharge time = 5 τ=50msec since the interval t2-t3 = 0.5 m sec. Thus, the capacitor will hold is a voltage.