FIELD EFFECT TRANSISTOR

A bipolar junction transistor (BJT) made as PNP or NPN is a current controlled device in which both electron current and hole current involved . the filed effect transistor (FET) is a unipolar device . It operates as a voltage controlled device with either electron current in an n-channel FET or hole current in a p-channel FET.

There are two categories c FET : the junction filed effect transistor (JFET) and the metal – oxide – semiconductor filed effect transistor (MOSFET) . the MOSFET category is further broken into : depletion and enhancement types .

A general comparison between FET and BJT devices can be mode :-

1- The FET has an extremely high input resistance about (100MΩ) typical , (BJT input resistance typically 2KΩ) .
2- The FET is less noisy than BJT and thus more suitable for input stages of low level amplifiers.
3- FET is more temperature stable then BJT.
4- FET is smaller then BJT.
5- FET is smaller gain bandwidth then BJT.
6- The BJT has a much higher sensitivity to changes in the applied signal then FET

JUNCTION FILED EFFECT TRANSISTOR (JFET)

The physical structure of a JFET is shown in fig (13.1) . The n-channel JFET shown in fig (13.1a) is constructed using a bar of n-type material into which a pair of p-type regions are diffused. A p-channel JFET is made using a bar of p-type material with n-type diffused region as shown in fig (13.1b). For the n-cannel JFET of fig (13.1a) the arrow at the gate shown the gate to be p-type material with channel n-type . The symbol for the p-channel JFET of fig (13.1b) includes an arrow at the gate showing the gate to be n-type material with channel p-type

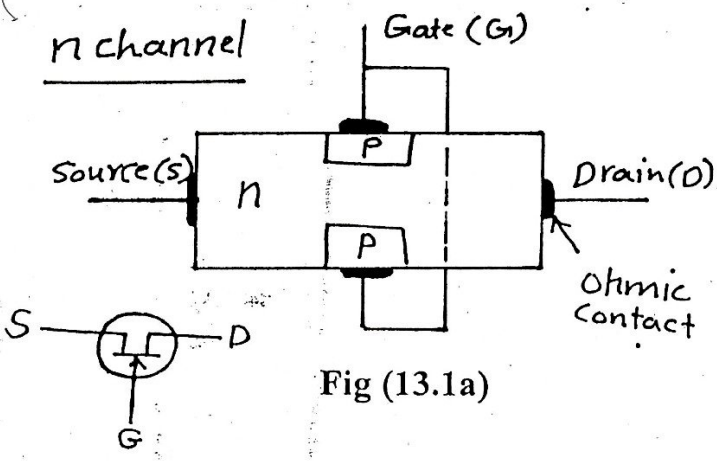
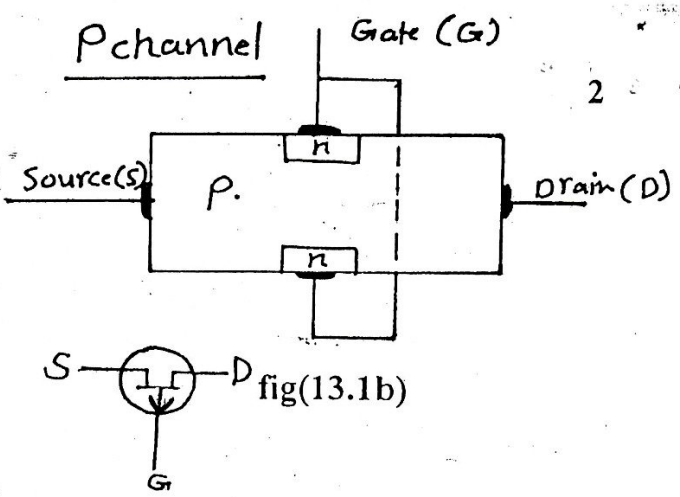


Fig (13.1a)



fig(13.1b)

JFET OPERATION

-To examine how the device is operated , consider the n-channel JFET of fug (13.2)shown with applied bias voltages to operate the device.

-the supply voltage ,V_{DD} provides a voltage across drain-source, V_{DS} which results in a current I_D from drain to source.

A voltage between gate and source,V_{GS} ,is set by a voltage supply V_{GG} .the effect of the gate –source voltage will be to create a depletion region in the channel and reduce the channel width to increase the drain source resistance resulting in less drain current

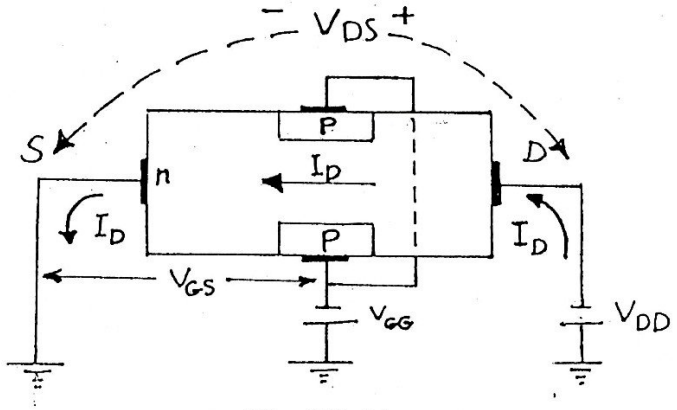


Fig (13.2)

Fig (13.3a) shows that a drain current through the n material of the drain source produces a voltage drop along the channel , which is more positive at the drain gate junction than at the source gate junction . this reverse bias potential across the p-n junction causes a depletion region to form as shown in fig (13.3a) .As the voltage ,V_{DD} is increased , the current ,I_D increases ,resulting in larger depletion region .

-Any further increase in V_{DD} will result in no increase in the drain current I_D then remaining constant. This operation is shown in fig (13.3c).

-As V_{DS} increases , the current I_D increases until the depletion region is fully formed across the channel , after which ,the drain current saturates and remains a constant value even for increased V_{DS} . this value of drain

current is referred to as I_{DSS} the drain to source current with , the gate source shorted .

-When V_{DS} is increased to a level where it appears that the two depletion region would touch a condition referred to as pinch-off will result. The level of V_{DS} that establishes this condition is referred as the pinch-off voltage V_P .

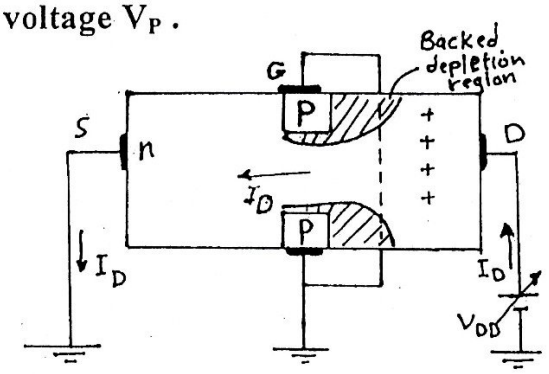


Fig (13.3a)

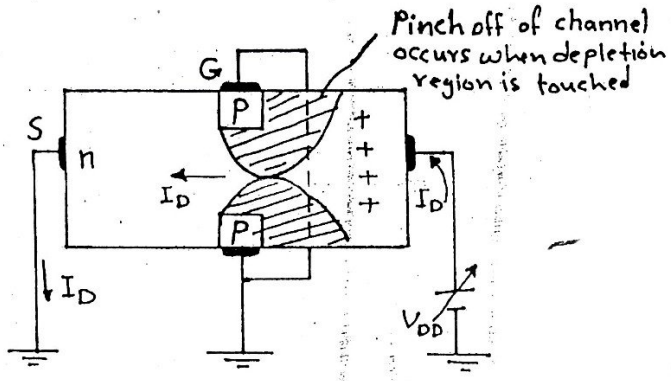
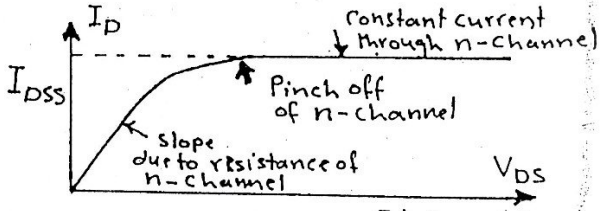


Fig (13.3b)



Fig(13.3c)

Fig(13.3)

DRAIN – SOURCE CARACTERISTIC

-Fig(13.4) shows a typical n-channel JFET drain –source characteristic .

-When V_{GS} =0V and V_{DS} <V_P (pinch-off voltage). I_d rises linearly with V_{DS} as shown in fig (13.4) this region is called ohmic region ,n-channel resistance is constant.

-When V_{GS} =0V and V_{DS} ≥V_P : I_D remain constant at its saturation value I_{DSS} beyond V_P .

-When V_{GS}<0 ,I_D increases as V_{DS} is increased until a saturation level is reached ,but this time at lower level then for V_{GS} =0V ,since the depletion region ,starting partly formed due to V_{GS} = -1V,fully forms at a lower level of drain –source current .

-Fig (13.5) shows a drain –source characteristic for a p-channel JFET with positive gate –source voltage reducing the drain –source current .

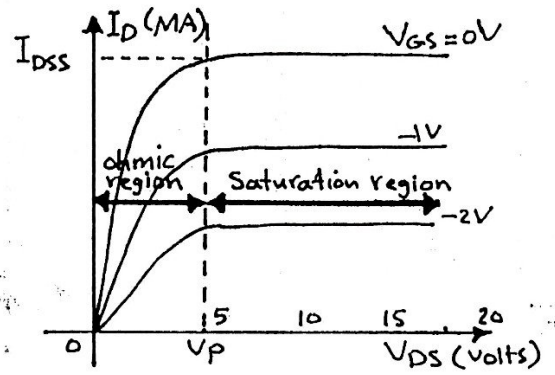


Fig (13.4)

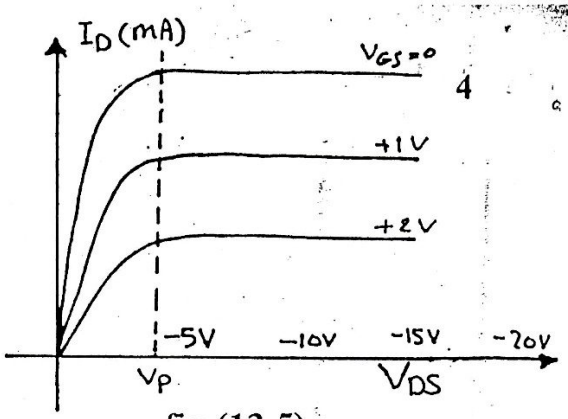


fig (13.5)

TRANSFER CHARACTERISTIC

- Transfer characteristic are plots of I_D versus V_{GS} for a fixed value of V_{DS} . The transfer characteristic can be obtained directly by measurement of device operation or draw from the drain characteristic as shown in fig (13.6) . Two important points of the transfer curve shown are the value of I_{DSS} and V_P .
- Transfer characteristic can be sketched to a satisfactory level of accuracy by using Shockley's equation (which represent the relationship between I_D and V_{GS})

$$I_D = I_{DSS}\,(1-\frac{V_{GS}}{V_P})^2 \ldots.(1)$$

V_{GS}	I_D
0	I_{DSS}
$0.3\,V_P$	$I_{DSS}/2$
$0.5\,V_P$	$I_{DSS}/4$
V_P	0

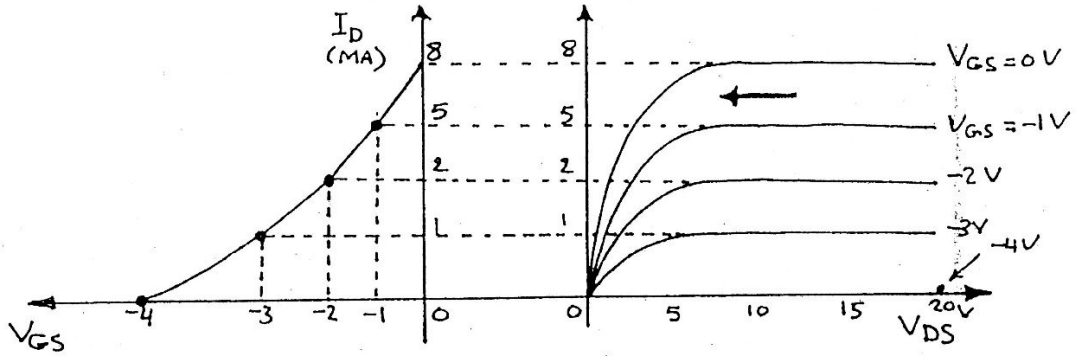


Fig (13.6)

EX (13.1) Determine the drain current of an n-channel JFET having pinch off voltage =-4V and drain –source saturation current =12mA at the following gate-source voltage a) V_{GS} =0V , b) V_{GS} =-1.2V

SOLUTION

Using Shockley's equation

a) $I_D = I_{DSS}(1-\frac{V_{GS}}{V_P})^2 = 12mA(1-\frac{0}{-4})^2 = 12mA$

b) $I_D = 12mA(1-\frac{-1.2}{-4})^2 = 5.88mA$

TRANSCONDUCTANCE FACTOR (gm)

-The change in drain current that will result from a change in gate –to source voltage .It is measured with drain-source shorted .

$gm = \frac{\Delta I_D}{\Delta V_{GS}}$ $|V_{DS} = 0$ .....(2)

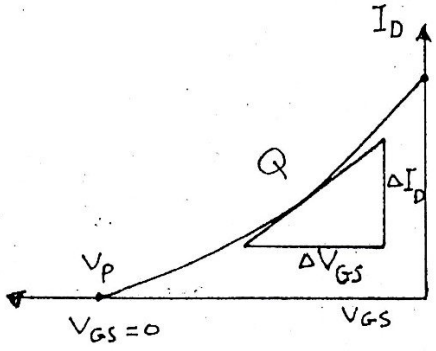
-The value of (gm) is measured in Siemens (s) or mho (1/Ω) with typical value (1ms to 10ms) .

-An equation for (gm) can be derived as follows

$I_D = I_{DSS}\ (1-\frac{V_{GS}}{V_P})^2$

$gm = \frac{\partial I_d}{\partial V_{GS}} = 2I_{DSS}\ (1-\frac{V_{GS}}{V_P})\ (\frac{-1}{V_P})$

$gm = \frac{2I_{DSS}}{|V_P|}\ (1-\frac{V_{GS}}{V_P})$



But g_{mo} is the value of (g m) at $V_{GS} = 0$

$gm = gmo\ (1-\frac{V_{GS}}{V_P})$ .....(3) where $gmo = \frac{2I_{DSS}}{|V_P|}$ .....(4)

EX(13.2) calculate the transconductance gm of a JFET having specified value of I_{DSS} =12mA and V_P =-4V at bias points a)V_{GS} =0V , b) V_{GS} =-1.5V

SOLUTION

Using eqs.(3,4)

$gm = gmo\ (1-\frac{V_{GS}}{V_P})$

where $gmo = \frac{2I_{DSS}}{|V_P|}$

$gmo = \frac{2(12mA)}{|-4V|} = \frac{24\times10^{-3}}{4} = 6\times10^{-3}S$

a) $gm = gmo\ (1-\frac{V_{GS}}{V_P}) = 6mS(1-\frac{0}{-4}) = 6mS$

b) $gm = 6mS(1-\frac{-1.5}{-4}) = 3.75mS$

FET BIASING

-DC bias of a FET device requires setting the gate source voltage , which result in a desired I_D (drain current) .
-For a JFET the drain current is limited by the saturation current ,I_{DSS}
-A depletion MOSFET can be biased below, at , or above I_{DSS}
-An enhancement MOSFET requires biasing at a gate source voltage greater then the threshold value to turn on the device.

1- FIXED BIAS

-since the FET has a high impedance seen looking into the gate (either reverse-biased p-n junction in a JFET or enhancement MOSFET) the dc voltage of the gate set by a voltage divider or fixed battery voltage is not affected or loaded by the FET
-Fixed bias is obtained using a battery to set the reverse bias voltage V_{GS} as in fig(11.1). Battery V_{GG} is used to set V_{GS} with no resulting current through R_G on the gate terminal . ($I_G = 0$) .
- R_G is included to allow any ac signal applied through capacitor C to develop across R_G
-Since the gate source is reversed biased, there is no current through that junction. No dc current passes through C so that no current result through R_G

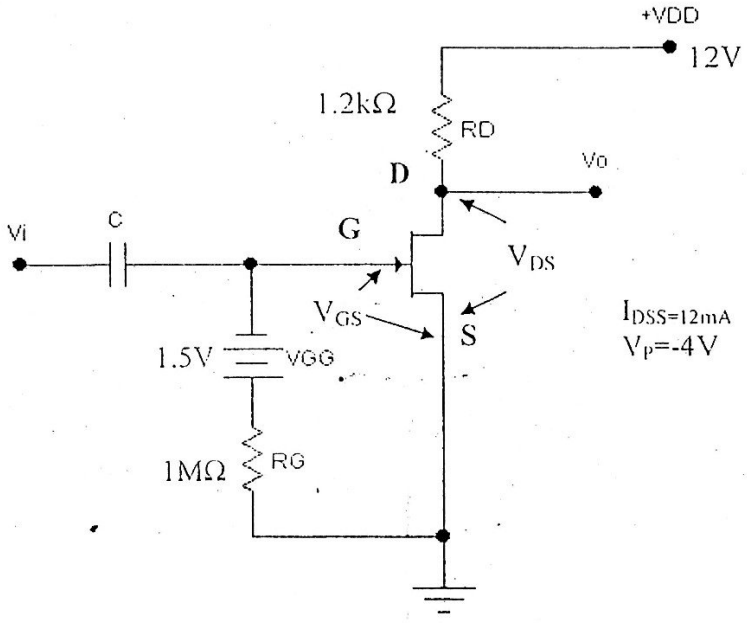


Fig.(14-1)

$$V_{RG} = I_G R_G = 0V$$

$$V_{GS} = V_G - V_S = V_{GG} - 0 = V_{GG} \quad \text{.....(14.1)}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{.....(14.2)}$$

$$V_{RD} = I_D R_D$$

$$V_D = V_{DD} - I_D R_D \quad \text{.....(14.3)}$$

EX(14.1) determine the drain current I_D and drain – source voltage V_{DS} for fig (14.1) if $R_D = 1.2K\Omega$, $V_{DD} = 12V$, $R_G = 1M\Omega$, $V_{GG} = 1.5V$, $I_{DSS} = 12mA$, $V_P = -4V$

SOLUTION

$V_{GS} = V_{GG} = -1.5V$

$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2 = 12mA(1 - \frac{-1.5}{-4})^2 \doteq 4.69mA$

$V_D = V_{DD} - I_D R_D = 12V - (4.69mA)(1.2K\Omega) = 6.4V$

$V_{DS} = V_D - V_S = 6.4 - 0 = 6.4V$

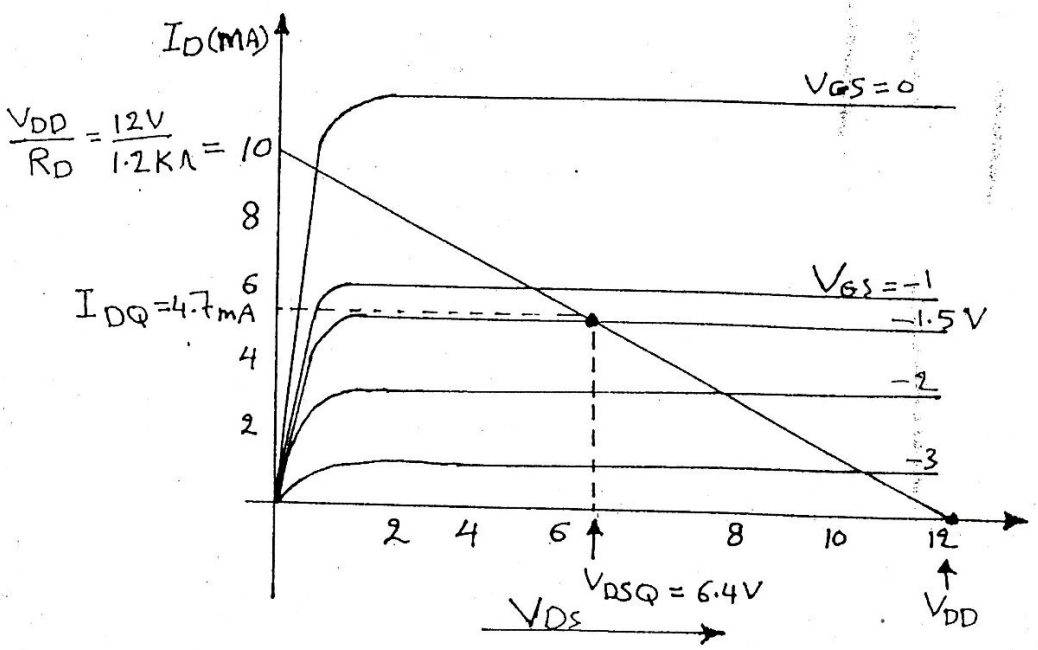
GRAPHICAL ANALYSIS USING JFET DRAIN – SOURCE CARACTERSTIC

-A dc load line representing the operation provided by equation (14.3) is drawn as following :-

$V_D = V_{DD} - I_D R_D$ .....(14.3)

If $I_D = 0 \rightarrow \therefore V_D = V_{DD}$

If $V_{DS} = V_D = 0 \rightarrow \therefore I_D = \frac{V_{DD}}{R_D}$



Fig(14.2)

EX(14.2) determine the operating point for the circuit of fig (14.1) using JFET whose drain characteristic is shown in fig (14.2)

SOLUTION

The dc load line is drawn by connecting the line between points

If $I_D = 0 \quad \therefore V_D = V_{DD} = 12V$

If $V_{DS} = 0 \quad \therefore I_D = \frac{V_{DD}}{R_D} = \frac{12V}{1.2K\Omega} = 10mA$

If V_{GS} = -1.5V , the operating point shown in fig(14.2) is at

$$I_{DQ} = 4.7mA \quad , \quad V_{DSQ} = 6.4V$$

2- JFET AMPLIFIER WITH SELF BIAS

-Using a source resistor R_S to provide the gate – source bias voltage without the need for a second supply voltage as shown in fig (14.3). since no gate current will pass through the reverse biased gate – source the gate current is

$$I_G = 0$$

$$V_G = I_G R_G = 0$$

$$V_S = I_D R_S \text{ .....(14.4)}$$

$$V_{GS} = V_G - V_S$$

$$= 0V - I_D R_S$$

$$V_{GS} = -I_D R_S \text{ .....(14.5)}$$

But $I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$ .....(eq 14.2)

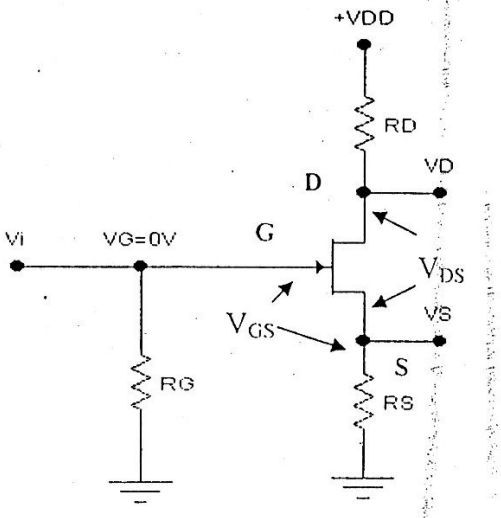


Fig.(14-3)

-Equation (14.2) and (14.5) can be saved mathematically to find I_D and V_{GS} .Graphical technique may be used to solve equations (14.2) and (14.5) as follow:-

1) Plot JFET transfer characteristic of eq (14.2)

2) Plot the straight line of eq (14.5) the self bias line by selecting two point of the line

If $I_D = 0 \rightarrow \therefore V_{GS} = 0$

$V_{GS} = V_P \rightarrow \therefore I_D = \frac{-V_P}{R_S}$

The intersection of the self bias line and the transfer characteristic provides the desired Q – point .

EX(14.3)

Determine the values of V_{GS} , I_D and V_{DS} for the circuit of fig (14.5) when, I_{DSS}=10mA and V_p=-4V.

SOLUTION

1)To plot the JFET transfer characteristic according to eq(14.2)

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

V_{GS} (V)	I_D(mA)
0	10 I_{DSS}
$(0.3V_P)$ - 1.2	5 $(I_{DSS}/2)$
$(0.5V_P)$ – 2	2.5 $(I_{DSS}/4)$
V_P - 4	0

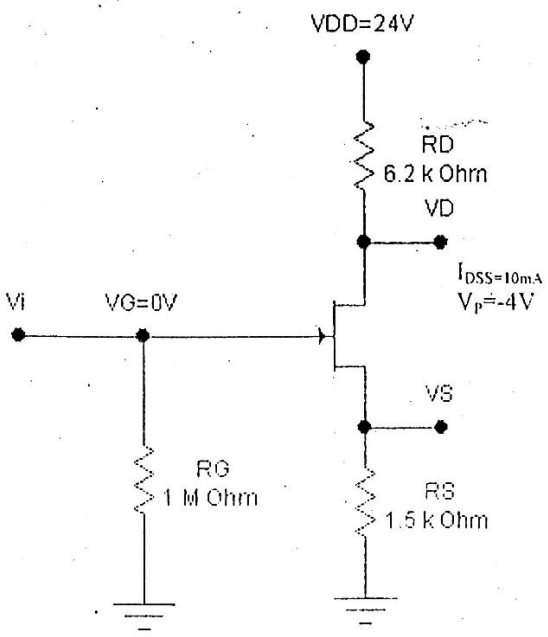


Fig.(14-5)

2) To plot the self bias line according to eq (14.5)

$V_{GS} = -I_D R_S$

V_{GS} (V)	I_D(mA)
0	0
$(-V_P/R_S)$ 2.64	(V_P) -4

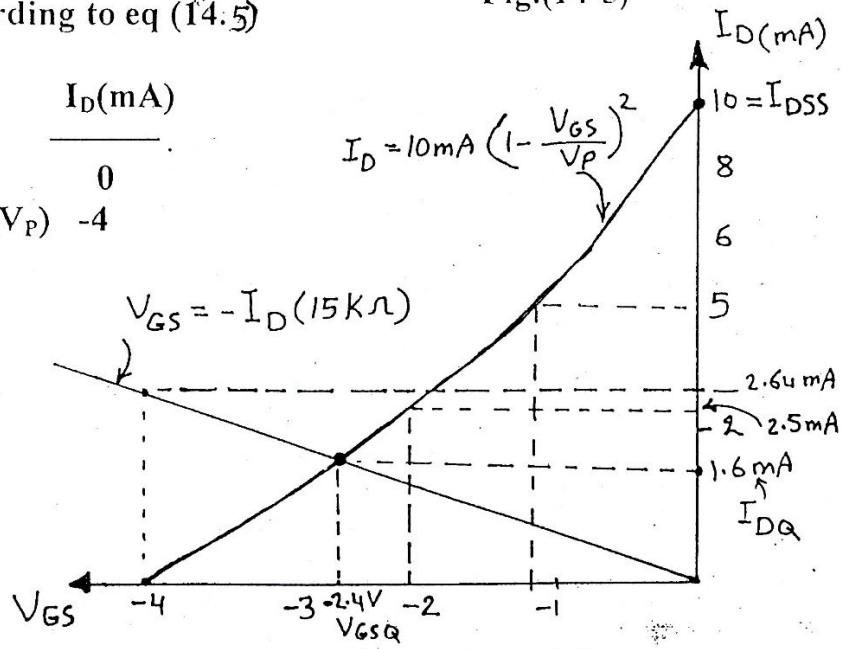


Fig.(14-6)

Fig (14.6) shown the plot of the transfer characteristic and self bias line with resulting dc bias at

$V_{GSQ} = -2.4V, I_{DQ} = 1.6mA$

$V_D = V_{DD} - I_D R_D = 24 - (1.6mA)(6.2) = 14V$

$V_S = I_D R_S = 1.6mA(1.5K\Omega) = 2.4V$

$\therefore V_{DS} = V_D - V_S = 14 - 2.4 = 11.6V$

3- VOLTAGE DIVIDER BIASING

- **The additional gate resistor R_G from gate to supply voltage as shown in fig (14.7) , results in greater adiustment of the dc bias point and permits larger value of R_S to be**

$$V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} V_{DD} \quad \text{.....(14.7)}$$

$I_G = 0$

$$V_{GS} = V_G - V_S = V_G - I_D R_S \quad \text{.....(14.8)}$$

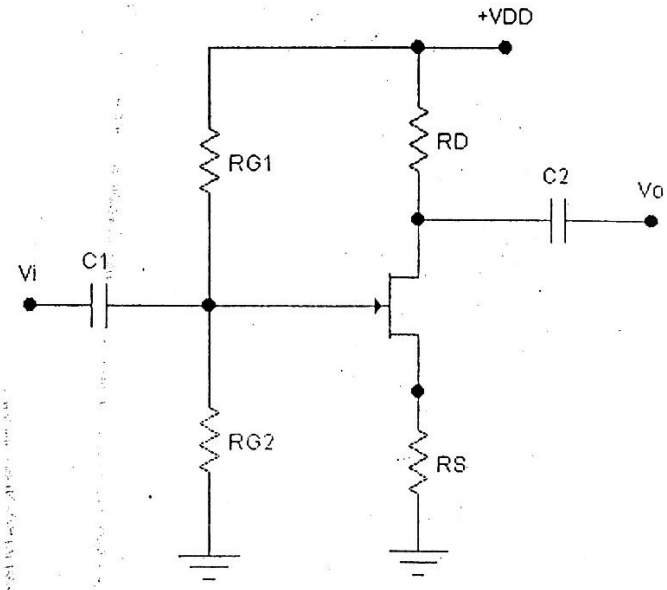


Fig.(14-7)

EX(14.5) Determine the bias current I_D and the bias voltage V_D , V_S , V_{DS} for circuit of fig (14.8). When I_{DSS}=8mA and V_p=-4V.

SOLUTION

The transfer characteristic is drawn by using the eq (14.2).

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

V_{GS} (V)	I_D(mA)
0	8 I_{DSS}
$(0.3V_P)$ - 1.2	4 $(I_{DSS}/2)$
$(0.5V_P)$ – 2	2 $(I_{DSS}/4)$
V_P - 4	0 0

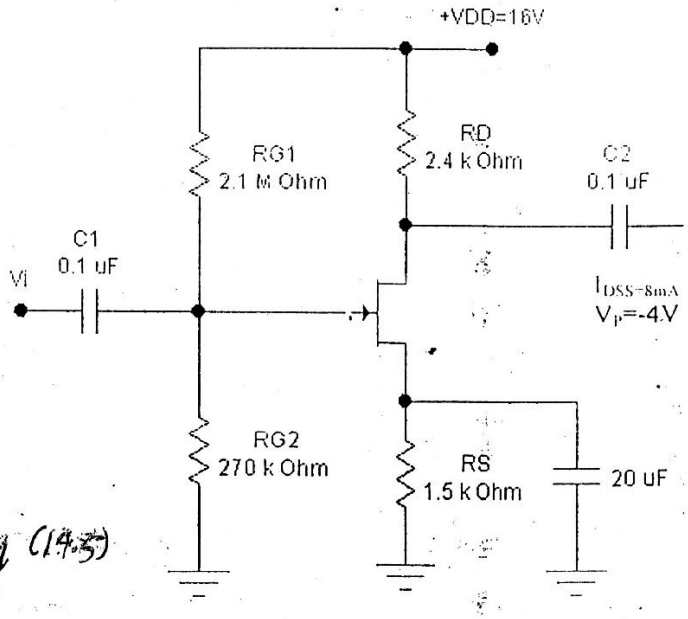


Fig.(14-8)

$$V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} V_{DD}$$

$$V_G = \frac{270K\Omega}{2.1M\Omega + 270K\Omega}(16V) = 1.82V$$

The self bias line is obtained using eq (14.5)

$$V_{GS} = V_G - V_S$$

$$V_{GS} = 1.82V - I_D(1.5K\Omega)$$

If

$I_D = 0 \rightarrow \therefore V_{GS} = 1.82\ V$

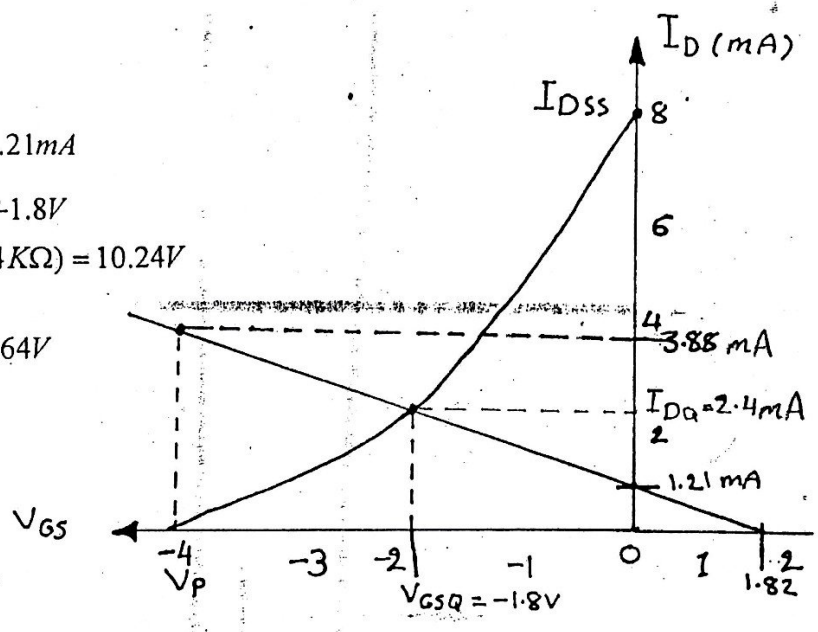
$V_{GS} = V_P \rightarrow \therefore I_D = \dfrac{1.82}{1.5K\Omega} = 1.21mA$

$I_{DQ} = 2.4mA \quad , \quad V_{DSQ} = 1.8V$

$V_D = V_{DD} - I_D R_D = 16V - (2.4mA)(2.4K\Omega) = 10.24V$

$V_S = I_D R_S = 2.4mA(1.5K\Omega) = 3.6V$

$\therefore V_{DS} = V_D - V_S = 10.24V - 3.6V = 6.64V$



FET SMALL SIGNAL ANALYSIS

-FET device can be used to build small signal amplifier cct providing voltage gain very high input resistance.

-Both JFET and depletion MOSFET can operate with similar dc bias , providing the same voltage gain . The MOSFET device however provides much higher input resistance .

-The common source amplifier configuration provides best voltage gain operation . An input signal is applied to the gate , and the output signal is taken from the drain , the source terminal being the reference or common .

-A common drain amplifier provides a noninverted output with near unity gain .

-A common gate amplifier connection is used less frequently , providing voltage gain with no polarity inversion .

-The FET ac equivalent cct is even simpler than that for a BJT , having only an output current source with value dependent on the device transconductance g_m .

-JFET and depletion MOSFET devices are often used in a linear circuit

-Enhancement MOSFET device are used in large scale integrated (LSI) , very large scale integrated (VLSI) and ultra large scale integrated (ULSI) .

JFET SMALL SIGNAL ANALYSIS

Fig (15.1) shows a simple equivalent circuit of FET . The ac voltage applied to the gate source , V_{gs} , results in a drain current I_d of value $g_m V_{gs}$. the device transconductance , g_m , relates the amount of current resulting from an applied voltage across gate source . The current source having value

$g_m V_{gs}$, is voltage controlled current source , since the current produce depends on the input voltage V_{gs}.

- Notice that there is an open circuit shown between the gate and source terminal . since the gate - to source junction is reverse biased in normal operation , the extremely large resistance between those terminals can be assumed to be infinite in most practical situations .

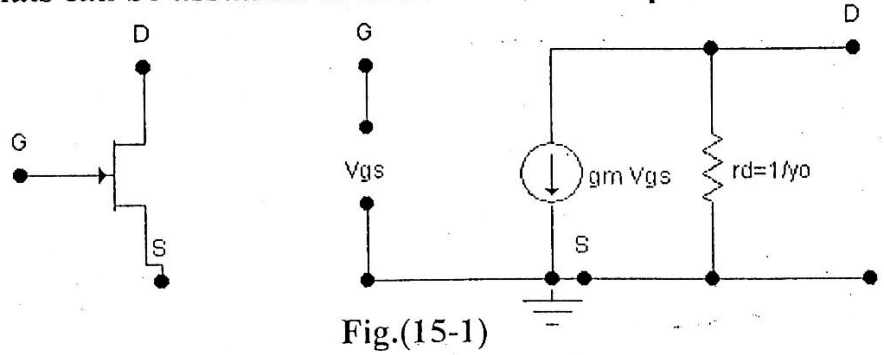


Fig.(15-1)

The value of g_m can be obtained from Shockley equation

$$gm = gmo\ (1 - \frac{V_{GS}}{V_P})^2 \quad .....(15.1)$$

where $gmo = \frac{2I_{DSS}}{V_P}$ (15.2) , r_d = output resistance

-The value of g_{mo} is the value tranconductance at V_{GS} = 0V bias and represents a fixed value of the maximum gain of the JFET device .

The small signal output resistance of a common source JFET is defined by

$$r_d = \frac{Vds}{id} = \frac{\Delta V_{DS}}{\Delta_{ID}} \Big|_{VGS = constant} \quad , \text{ ohm's} \quad ....(15.3)$$

This parameter is also called the drain resistance r_d or r_{ds} . This output resistance is usually listed on specification sheets as

Y_{OS} = small – signal output conductance

-To demonstrate use of the ac equivalent circuit , consider the FET amplifier cct of fig (15.2a) . The ac equivalent cct is drawn in fig (15.2b) with capacitors replaced by a short for ac operation and with the FET device replaced by its simple equivalent cct (r_d assumed infinite or open cct).

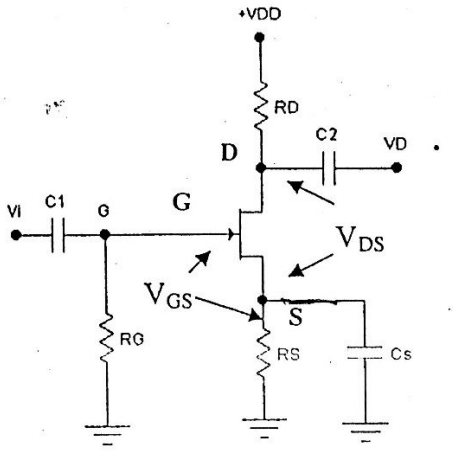


Fig (15.2a)

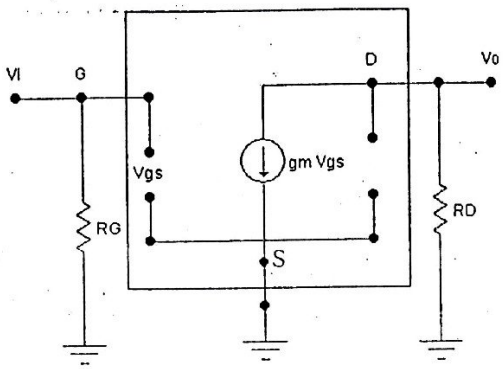


Fig (15.2b)

$V_O = -I_d R_D = - \ g_m V_{gs} R_D$ .....(15.4)

But $V_i = V_{gs}$

$\therefore A_V = \dfrac{V_O}{V_i} = - V_{gs} R_D$.....(15.5)

$R_i = R_G$ .....(15.6)

$R_O = R_D$ .....(15.7)

-The voltage gain equation can be written in a modified from by identifying a resistance

$r_m = \dfrac{1}{g_m}$ .....(15.8a)

$\therefore A_V = -g_m R_D = -\dfrac{R_D}{r_m}$ .....(15.8b)

There is a similarity between the JFET ac resistance ,r_m , at the dc bias voltage V_{GS} and the BJT ac resistance ,r_e at the bias current I_E .

EX(15.1) Calculate A_V ,R_i and R_o for the JFET amplifier of fig (15.3a) (ignore r_d) .When I_{DSS}=8mA and V_p=-4V.

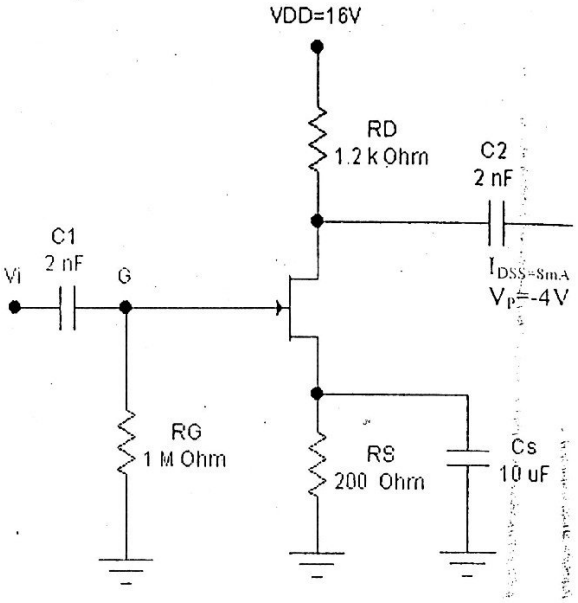


Fig.(15-3a)

SOLUTION

DC analysis to find V_{GS}

1)plot the JFET transfer characteristic using Eq(14-2)

$$I_D = I_{DSS}(1-\frac{V_{GS}}{V_P})^2$$

V_{GS} (V)	I_D(mA)
0	8 I_{DSS}
$(0.3V_P)$ - 1.2	4 $(I_{DSS}/2)$
$(0.5V_P)$ – 2	2 $(I_{DSS}/4)$
V_P - 4	0 0

2)plot the self bias line $V_{GS} = -I_DR_S$

$V_G = 0V$
$V_S = I_DR_S$
$V_{GS} = V_G - V_S$
$=-I_DR_S$

V_{GS} (V)		I_D(mA)	
0		0	
$(-V_P/R_S)$	20	$(-V_P)$	4

Fig (15.3b) shows the plot of the transfer characteristic and self bias lines with resulting dc bias at V_{GS} = -0.94V using Eqs (15.1 , 15.2)

$$gmo = \frac{2I_{DSS}}{|V_P|} = \frac{2\times 8mA}{|-4V|} = 4mS$$

$$gm = gmo\,(1-\frac{V_{GS}}{V_P})^2 = 4mS(1-\frac{0.94V}{-4V})^2 = 3.06mS$$

Using Eqs (15.5 , 15.6 , 15.7)

$$\therefore A_V = -g_m R_D = -(3.06mS)(1.2k\Omega) = -3.67$$

$R_i = R_G$ =1MΩ

$R_o = R_D$ =1.2KΩ

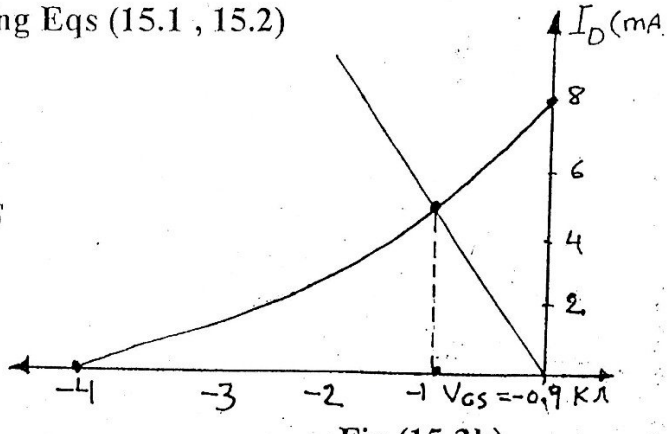


Fig.(15-3b)

1- AMPLIFIER WITH SOURCE RESISTANCE

-If the amplifier is built with part of the source resistance unbypassed , the relation for voltage gain can be determined using the ac equivalent cct of fig (15.4a) (the output resistance , r_d , considered negligible) .

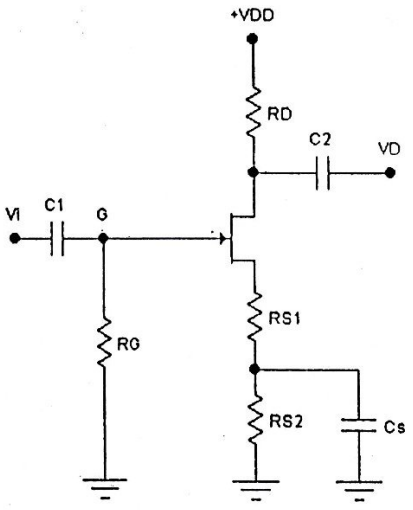


Fig (15-4b)

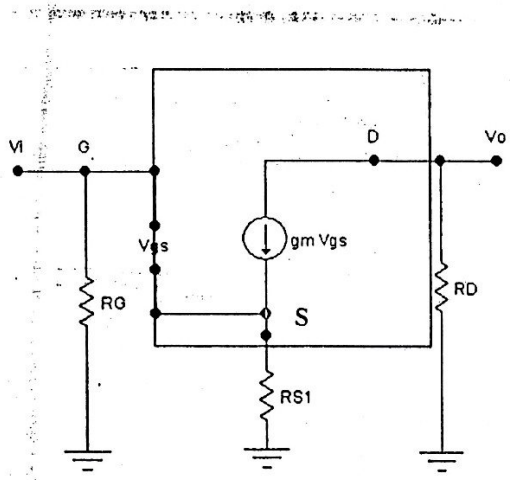


Fig (15-4a)

$V_{gs} = V_G - V_S = V_i - I_d R_{S1} = V_i - g_m V_{gs} R_{S1}$

$\therefore V_i = (1 + g_m R_{S1})\, V_{gs} \quad \rightarrow \quad V_{gs} = V_i / 1 + g_m R_{S1}$

$V_O = - I_d R_D = -g_m V_{gs} R_D = - g_m R_D\, V_i / 1 + g_m R_{S1}$

So that

$$A_V = \frac{V_O}{Vi} = \frac{-g_m R_D}{1 + g_m R_{S1}} \quad .....(15.9)$$

Using eq (15.8a)

$$r_m = \frac{1}{g_m}$$

$$\therefore A_V = -\frac{(\frac{1}{r_m})R_D}{1 + (\frac{1}{r_m})R_{S1}} = \frac{R_D}{r_m + R_{S1}} \quad .....(15.10)$$

EX(15.3) **for the network shown in fig (15.7)**
a)find expressions for A_V ,R_i and R_o (ignore r_d)
b)calculate A_V ,R_i and R_o When I_{DSS}=8mA and V_p=-4V.

SOLUTION

1)plot the JFET transfer charàcteristic

$$I_D = I_{DSS}(1-\frac{V_{GS}}{V_P})^2$$

V_{GS} (V)	I_D(mA)
0	8 I_{DSS}
$(0.3V_P)$ - 1.2	4 $(I_{DSS}/2)$
$(0.5V_P)$ – 2	2 $(I_{DSS}/4)$
V_P - 4	0 0

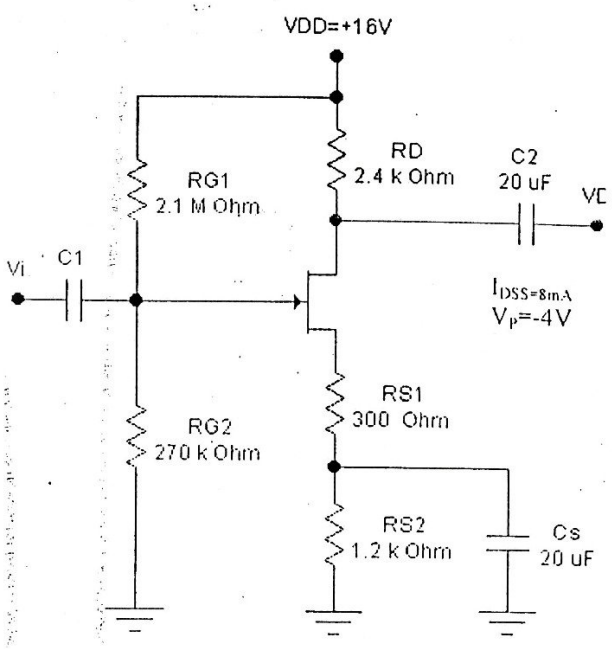


Fig.(15-7a)

2) plot the self bias line
The gate is reverse biased so that $I_G = 0$, the gate voltage V_G is

$$V_G = \frac{R_{G2}}{R_{G1}+R_{G2}}V_{DD} = \frac{270K\Omega}{2.1M\Omega+270K\Omega}16V = 1.821$$

$V_{GS} = V_G - V_S = V_G - I_d(R_{S1} + R_{S2})$
$=1.28V - I_d(0.3K\Omega + 1.2K\Omega)$
$V_{GS} = 1.28V - I_d(1.5K\Omega)$
If
$I_D = 0 \rightarrow \therefore V_{GS} = 1.82$

$$V_{GS} = 0 \rightarrow \therefore I_D = \frac{1.82}{1.5K\Omega} = 1.21mA$$

From fig (15.7a) , the dc bias V_{GSQ} =-1.8V

$$gm = gmo\,(1-\frac{V_{GSQ}}{V_P})$$

$$gm = \frac{2I_{DSS}}{|V_P|}\,(1-\frac{V_{GSQ}}{V_P})$$

$$gm = \frac{2(8mA)}{|-4V|}\,(1-\frac{-1.8V}{-4V}) = 2.2mS$$

$$r_m = \frac{1}{g_m} = \frac{1}{2.2\times10^{-3}} = 454.5\Omega$$

$$A_V = -\frac{R_D}{r_m+R_{S1}} = \frac{-2.4\times10^3}{454.5+300} = -3.18$$

$R_i = R_{G1} /\!/ R_{G2} = 2.1M\Omega /\!/ 270K\Omega = 239K\Omega$
$R_o = R_D = 2.4K\Omega$

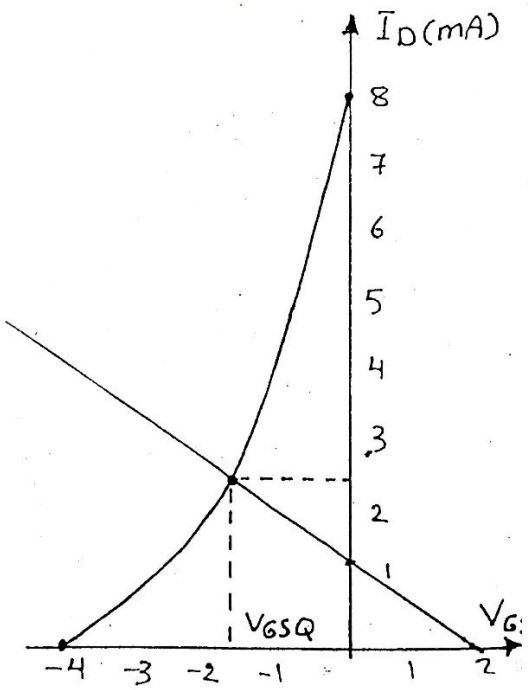
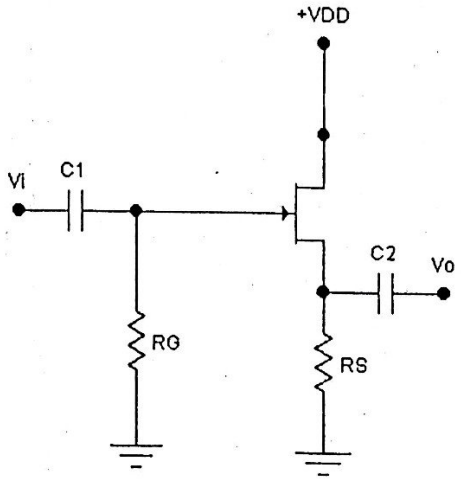
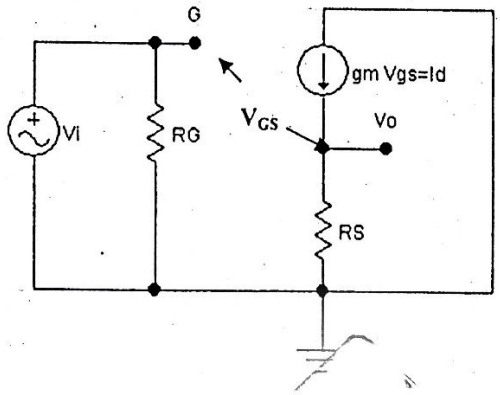


Fig.(15-7b)

2-SOURCE FOLLOWER (COMMON DRAIN) CIRCUIT

- The voltage gain for source follower is less than unity with no polarity inversion (change) and the cct . provides high input resistance and lower output resistance than common source configuration . Fig (15.11) shown the source follower .





$Vgs = V_i - V_o$

But

$V_O = -I_d R_S = -g_m V_{gs} R_S$

$Vgs = V_i - I_d R_S$

$Vgs = V_i - g_m V_{gs} R_S$

$V_i = (1 + g_m R_{S1})\, V_{gs}$

$$A_V = \frac{V_O}{Vi} = \frac{g_m V_{gs} R_S}{(1+g_m R_S) V_{gs}} = \frac{g_m R_S}{1+g_m R_S} \quad \text{.....(15.16)}$$

Using $r_m = \frac{1}{g_m}$

$$\therefore A_V = \frac{(\frac{1}{r_m}) R_S}{1+(\frac{1}{r_m}) R_S} = \frac{R_S}{r_m + R_S}$$

$R_i = R_G$ ..... (15.18)

$R_o = R_S // r_m$ ..... (15.19)

(the o/p resistance is the source resistance // device ac resistance)

EX(15.6)

For the network shown in fig (15.12)
a)find expressions for A_V ,R_i and R_o
b)calculate A_V ,R_i and R_o

SOLUTION

1) plot the transfer characteristic

$$I_D = I_{DSS}(1-\frac{V_{GS}}{V_P})^2$$

V_{GS} (V)	I_D(mA)
0	16 I_{DSS}
$(0.3V_P)$ - 1.2	8 $(I_{DSS}/2)$
$(0.5V_P)$ – 2	4 $(I_{DSS}/4)$
V_P - 4	0 0

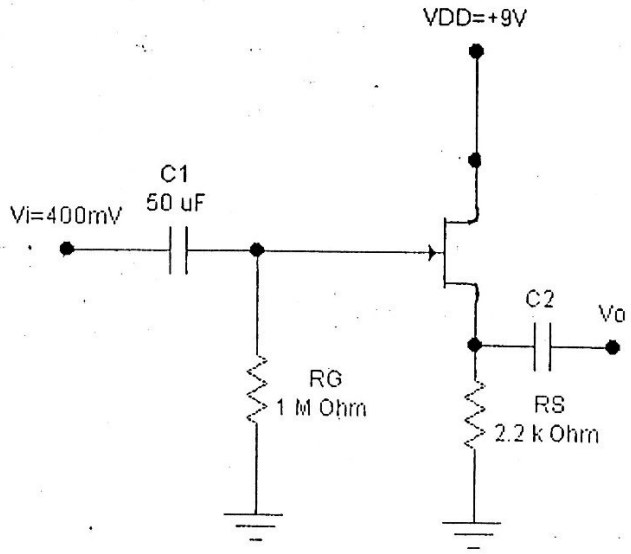


Fig.(15-12a)

2) plot the self bias line

$V_{GS} = -I_D R_S$

If

$I_D = 0 \rightarrow \therefore V_{GS} = 0$

If

$V_{GS} = V_P = -4 \quad \therefore I_D = \frac{+4}{2.2K\Omega} = 1.8mA$

∴ the intersection of transfer characteristic and self bias line is

V_{GS} = -2.86V

$$gmo = \frac{2I_{DSS}}{|V_P|} = \frac{2\times16\times10^{-3}}{|-4|} = 8mS$$

$$gm = gmo\,(1-\frac{V_{GS}}{V_P}) = 8(1-\frac{-2.86}{-4}) = 2.3mS$$

JFET ac resistance = $r_m = \frac{1}{g_m} = \frac{1}{2.3mS} = 434.4\Omega$

$$A_V \fallingdotseq \frac{R_S}{r_m + R_S} = \frac{2.2\times10^3}{434.4 + 2.2\times10^3} = 0.835$$

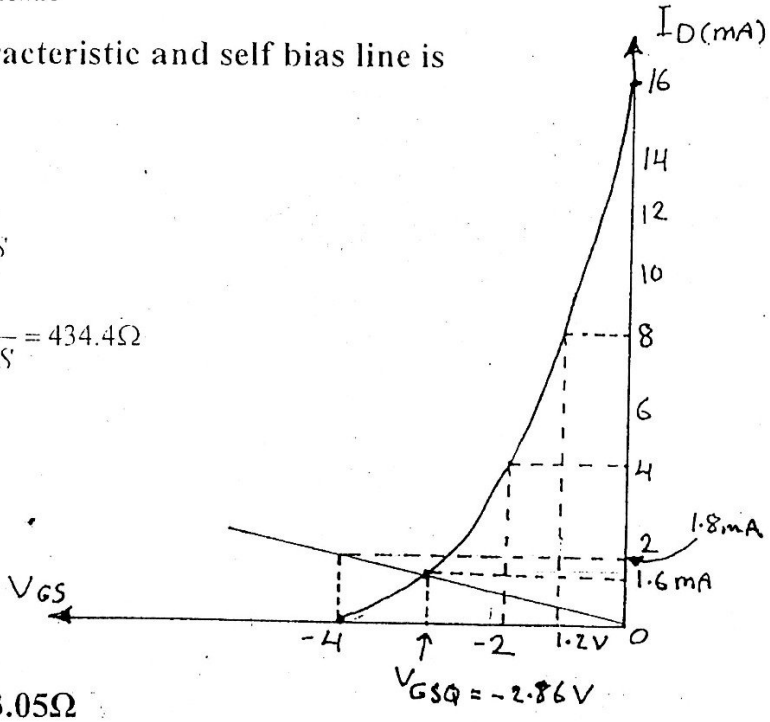


Fig.(15-12b)

$R_i = R_G$=1MΩ

$R_o = R_S // r_m$ = 434.4Ω//2.2KΩ = 363.05Ω

3- COMMON GATE CIRCUIT

A third configuration is shown in fig (15.15) with ac input to source , ac output form drain – this circuit being the common gate amplifier configuration . this amplifier form has low input resistance , noninverting voltage gain (similar in magnitude to a common drain) ,and output resistance the same an the common drain .
The ac equivalent for the circuit of fig (15.15a) is drawn in fig (15.15b) .

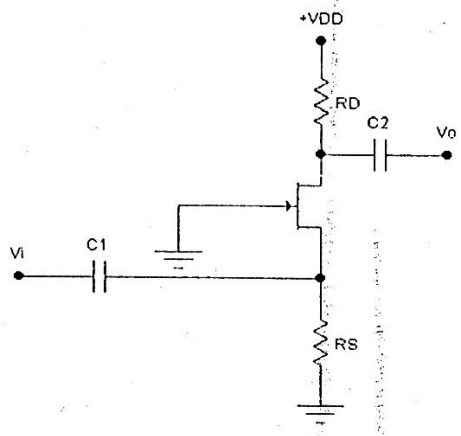


Fig (15.15a)

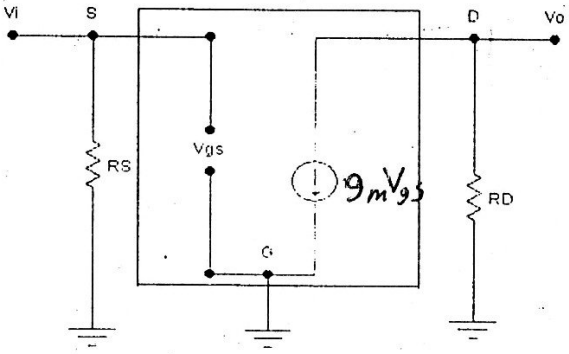


fig (15.15b)

$V_O = - I_d R_D = -g_m V_{GS} R_D = - g_m R_D (-V_i)$

$\therefore A_V = \frac{V_O}{Vi} = g_m R_D = \frac{R_D}{r_m}$ ....(15.24)

$R_i = R_S$ ..... (15.25)

$R_o = R_D$ ..... (15.26)

EX15.8 calculate V_o for the network of fig (15.15) if $R_S = 1.1K\Omega$, $R_D = 3.6K\Omega$, $I_{DSS} = 10mA$, $V_P = -4V$ and $V_i = 100m\ V_{rms}$

SOLUTION

1) plot the transfer characteristic

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2 = 10mA(1 - \frac{V_{GS}}{-4})^2$$

2) plot the self bias line

$V_{GS} = -R_S I_D = -1.1(K\Omega) I_d(mA)$

$\therefore$ Dc bias $V_{GSQ} = -2.2V$

$$gmo = \frac{2I_{DSS}}{|V_P|} = \frac{2 \times 10mA}{|-4|} = 5mS$$

$$gm = gmo\ (1 - \frac{V_{GS}}{V_P}) = 5(1 - \frac{-2.2V}{-4}) = 2.25mS$$

$$\therefore A_V = \frac{R_D}{r_m} = g_m R_D = 2.25mS(3.6K\Omega) = 8.1$$

$V_o = A_V V_i = 8.1(100mV_{rms}) = 0.81V_{rms}$