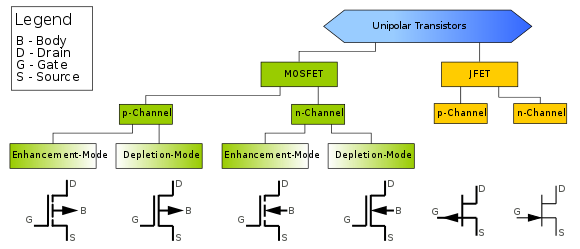
**FETTransistor) unipolar transistor(**

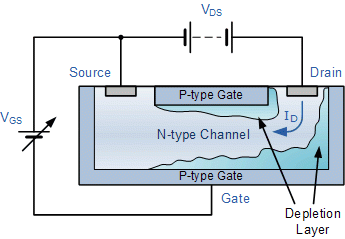
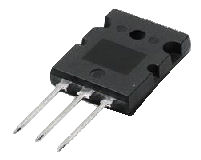
unipolar transistors are two main types of field effect transistor, the **Junction Field Effect Transistor** or JFET and the **Metal Oxide Semiconductor Field Effect Transistor** or MOSFET . 

1. Junction Field Effect Transistor (JFET)

The Junction Field Effect Transistor, or JFET, is a voltage controlled three terminal unipolar semiconductor devices available in N-channel and P-channel configurations.

In the Bipolar Junction Transistor (BJT) output Collector current of the transistor is proportional to input current flowing into the Base terminal of the device, thereby making the bipolar transistor a “CURRENT” operated device (Beta model) as a smaller current can be used to switch a larger load current.

The **Field Effect Transistor** (**FET**), uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the **Field Effect Transistor** a “VOLTAGE” operated device.



Typical Field Effect Transistor

The Field Effect Transistor has very similar characteristics to those of their Bipolar Transistor counterparts. For example, high efficiency, instant operation, robust and cheap and can be used in most electronic circuit applications to replace their equivalent bipolar junction transistors (BJT).

Field effect transistors can be made much smaller than an equivalent BJT transistor and along with their low power consumption and power dissipation makes them ideal for use in integrated circuits such as the CMOS range of digital logic chips.

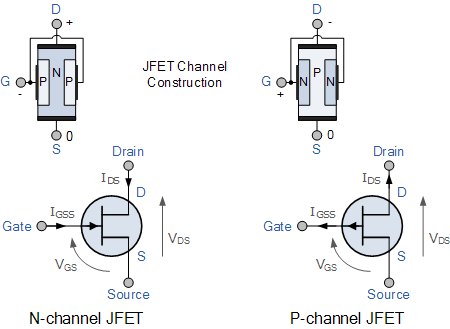
The **Field Effect Transistor** has one major advantage over its standard bipolar transistor, in that their input impedance, ( Rin ) is very high, (thousands of Ohms), while the BJT is comparatively low. This very high input impedance makes them very sensitive to input voltage signals, but the price of this high sensitivity also means that they can be easily damaged by static electricity.

The relationship between the connections of a junction field effect transistor and a bipolar junction transistor are compared below.

**Comparison of Connections between a JFET and a BJT**

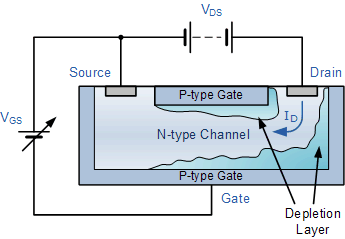
|  |  |
| --- | --- |
| Bipolar Transistor (BJT) | Field Effect Transistor (FET) |
| Emitter – (E)     >>     Source – (S) | |
| Base – (B)     >>     Gate – (G) | |
| Collector – (C)     >>     Drain – (D) | |

The symbols and basic construction for both configurations of JFETs are shown below.



The semiconductor “channel” of the Junction Field Effect Transistor is a resistive path through which a voltage VDS causes a current ID to flow. The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive.

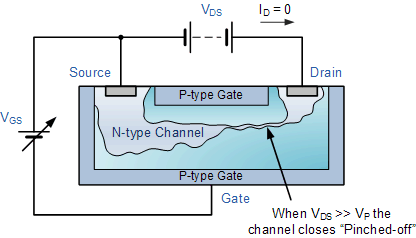
Biasing of an N-channel JFET



With no external Gate voltage ( VG = 0 ), and a small voltage ( VDS ) applied between the Drain and the Source, maximum saturation current ( IDSS ) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions.

If a small negative voltage ( -VGS ) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, Since the PN-junction is reverse biased, little current will flow into the gate connection. As the Gate voltage ( -VGS ) is made more negative, the width of the channel decreases until no more current flows between the Drain and the Source and the FET is said to be “pinched-off” (similar to the cut-off region for a BJT). The voltage at which the channel closes is called the “pinch-off voltage”, ( VP ).

In this pinch-off region the Gate voltage, VGS controls the channel current and VDS has little or no effect.

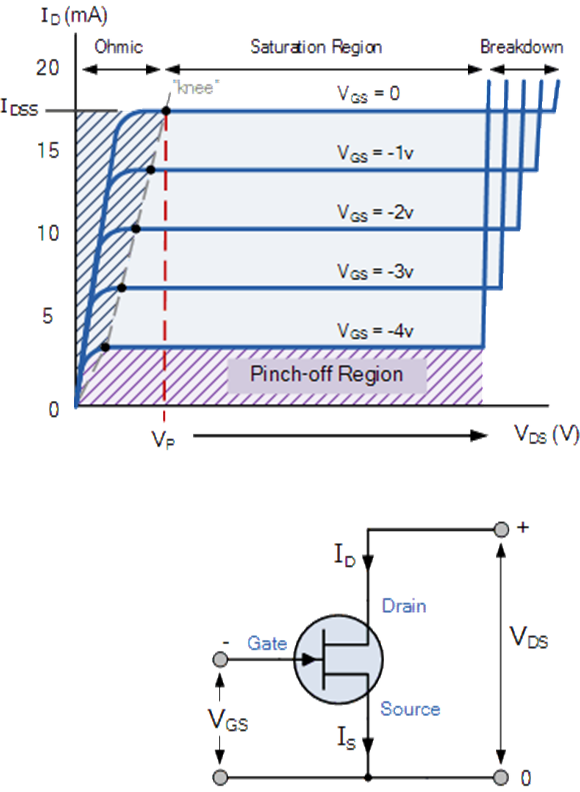




JFET Model

The result is that the FET acts more like a voltage controlled resistor which has zero resistance when VGS = 0 and maximum “ON” resistance ( RDS ) when the Gate voltage is very negative. Under normal operating conditions, the JFET gate is always negatively biased relative to the source.

Output characteristic V-I curves of a typical junction FET



Because a Junction Field Effect Transistor is a voltage controlled device, “NO current flows into the gate” then the Source current ( IS ) flowing out of the device equals the Drain current flowing into it and therefore ( ID = IS ).

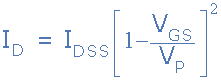
The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

* Ohmic Region – When VGS = 0 the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.
* Cut-off Region – This is also known as the pinch-off region were the Gate voltage, VGS is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
* Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, ( VGS ) while the Drain-Source voltage, ( VDS ) has little or no effect.
* Breakdown Region – The voltage between the Drain and the Source, ( VDS ) is high enough to causes the JFET’s resistive channel to break down and pass uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current ID decreases with an increasing positive Gate-Source voltage, VGS.

The Drain current is zero when VGS = VP. For normal operation, VGS is biased to be somewhere between VP and 0. Then we can calculate the Drain current, ID for any given bias point in the saturation or active region as follows:

Drain current in the active region.



Note that the value of the Drain current will be between zero (pinch-off) and IDSS (maximum current). By knowing the Drain current ID and the Drain-Source voltage VDS the resistance of the channel ( RDS ) is given as:

Drain-Source Channel Resistance.

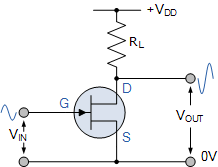
junction field effect transistor channel resistance

Where: gm is the “transconductance gain” since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

**Modes of FET’s**

Like the bipolar junction transistor, the field effect transistor being a three terminal device is capable of three distinct modes of operation and can therefore be connected within a circuit in one of the following configurations.

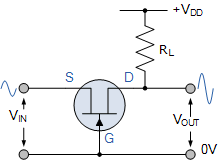
**Common Source (CS) Configuration**



In the **Common Source** configuration (similar to common emitter), the input is applied to the Gate and its output is taken from the Drain as shown. This is the most common mode of operation of the FET due to its high input impedance and good voltage amplification and as such Common Source amplifiers are widely used.

The common source mode of FET connection is generally used audio frequency amplifiers and in high input impedance pre-amps and stages. Being an amplifying circuit, the output signal is 180o “out-of-phase” with the input.

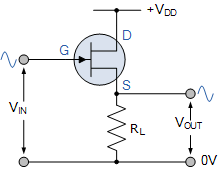
**Common Gate (CG) Configuration**



In the **Common Gate** configuration (similar to common base), the input is applied to the Source and its output is taken from the Drain with the Gate connected directly to ground (0v) as shown. The high input impedance feature of the previous connection is lost in this configuration as the common gate has a low input impedance, but a high output impedance.

This type of FET configuration can be used in high frequency circuits or in impedance matching circuits were a low input impedance needs to be matched to a high output impedance. The output is “in-phase” with the input.

**Common Drain (CD) Configuration**



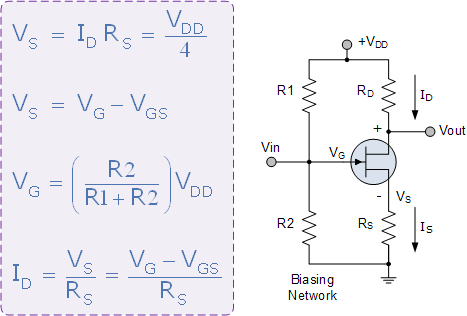
In the **Common Drain** configuration (similar to common collector), the input is applied to the Gate and its output is taken from the Source. The common drain or “source follower” configuration has a high input impedance and a low output impedance and near-unity voltage gain so is therefore used in buffer amplifiers. The voltage gain of the source follower configuration is less than unity, and the output signal is “in-phase”, 0o with the input signal.

This type of configuration is referred to as “Common Drain” because there is no signal available at the drain connection, the voltage present, +VDD just provides a bias. The output is in-phase with the input.

**The JFET Amplifier**

Just like the bipolar junction transistor, JFET’s can be used to make single stage class A amplifier circuits with the JFET common source amplifier and characteristics being very similar to the BJT common emitter circuit. The main advantage JFET amplifiers have over BJT amplifiers is their high input impedance which is controlled by the Gate biasing resistive network formed by R1 and R2 as shown.

**Biasing of JFET Amplifier**

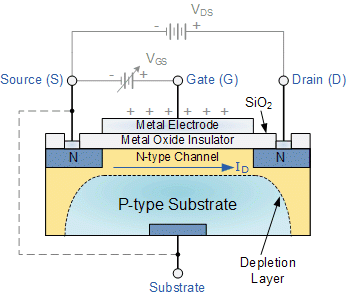


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The control of the Drain current by a negative Gate potential makes the **Junction Field Effect Transistor** useful as a switch and it is essential that the Gate voltage is never positive for an N-channel JFET. The principals of operation for a P-channel JFET are the same as for the N-channel JFET, except that the polarity of the voltages need to be reversed.

2. **Metal Oxide Semiconductor Field Effect Transistor** (MOSFET)

MOSFET’s operate the same as JFET’s but have a gate terminal that is electrically isolated from the conductive channel.



As well as the Junction Field Effect Transistor (JFET), there is another type of Field Effect Transistor available whose Gate input is electrically insulated from the main current carrying channel and is therefore called an **Insulated Gate Field Effect Transistor**.

The most common type of insulated gate FET which is used in many different types of electronic circuits is called the **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.

The **MOSFET** is a voltage controlled field effect transistor that differs from a JFET in that it has a “Metal Oxide” Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.

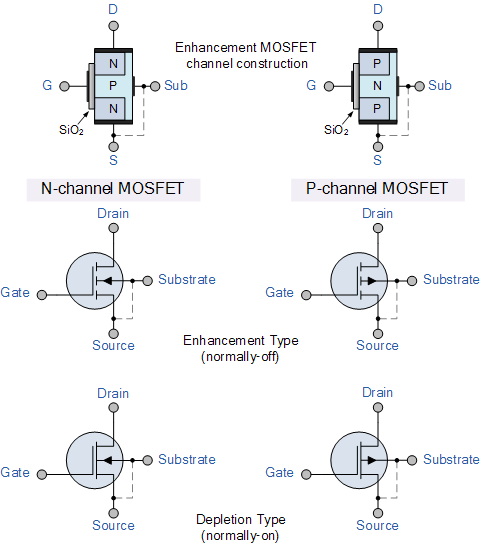
This ultra-thin insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the **MOSFET** extremely high way up in the Mega-ohms ( MΩ ) region thereby making it almost infinite.

As the Gate terminal is electrically isolated from the main current carrying channel between the drain and source, “NO current flows into the gate” and just like the JFET, the MOSFET also acts like a voltage controlled resistor where the current flowing through the main channel between the Drain and Source is proportional to the input voltage. Also like the JFET, the MOSFETs very high input resistance can easily accumulate large amounts of static charge resulting in the **MOSFET** becoming easily damaged unless carefully handled or protected.

Like the previous JFET tutorial, MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:

* Depletion Type   –   the transistor requires the Gate-Source voltage, ( VGS ) to switch the device “OFF”. The depletion mode MOSFET is equivalent to a “Normally Closed” switch.
* Enhancement Type   –   the transistor requires a Gate-Source voltage, ( VGS ) to switch the device “ON”. The enhancement mode MOSFET is equivalent to a “Normally Open” switch.

The symbols and basic construction for both configurations of MOSFETs are shown below.



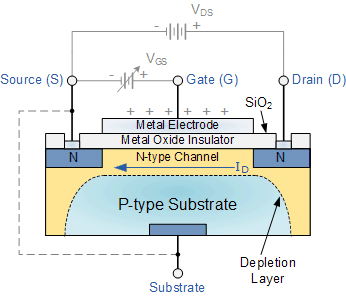
The four MOSFET symbols above show an additional terminal called the Substrate and is not normally used as either an input or an output connection but instead it is used for grounding the substrate. It connects to the main semiconductive channel through a diode junction to the body or metal tab of the MOSFET.

Usually in discrete type MOSFETs, this substrate lead is connected internally to the source terminal. When this is the case, as in enhancement types it is omitted from the symbol for clarification.

The line in the MOSFET symbol between the drain (D) and source (S) connections represents the transistors semiconductive channel. If this channel line is a solid unbroken line then it represents a “Depletion” (normally-ON) type MOSFET as drain current can flow with zero gate biasing potential.

If the channel line is shown as a dotted or broken line, then it represents an “Enhancement” (normally-OFF) type MOSFET as zero drain current flows with zero gate potential. The direction of the arrow pointing to this channel line indicates whether the conductive channel is a P-type or an N-type semiconductor device.

**Basic MOSFET Structure and Symbol**



The construction of the Metal Oxide Semiconductor FET is very different to that of the Junction FET. Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge carriers, electrons for n-channel or holes for P-channel, through the semiconductive drain-source channel. The gate electrode is placed on top of a very thin insulating layer and there are a pair of small n-type regions just under the drain and source electrodes.

We saw in the previous tutorial, that the gate of a junction field effect transistor, JFET must be biased in such a way as to reverse-bias the pn-junction. With a insulated gate MOSFET device no such limitations apply so it is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve).

This makes the MOSFET device especially valuable as electronic switches or to make logic gates because with no bias they are normally non-conducting and this high gate input resistance means that very little or no control current is needed as MOSFETs are voltage controlled devices. Both the p-channel and the n-channel MOSFETs are available in two basic forms, the **Enhancement** type and the **Depletion** type.

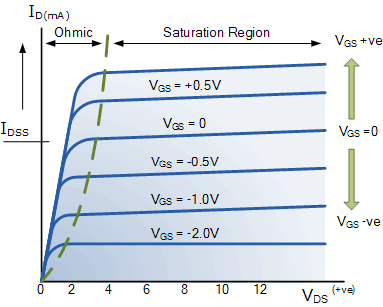
**Depletion-mode MOSFET**

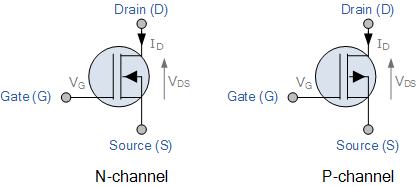
The **Depletion-mode MOSFET**, which is less common than the enhancement mode types is normally switched “ON” (conducting) without the application of a gate bias voltage. That is the channel conducts when VGS = 0 making it a “normally-closed” device. The circuit symbol shown above for a depletion MOS transistor uses a solid channel line to signify a normally closed conductive channel.

For the n-channel depletion MOS transistor, a negative gate-source voltage, -VGS will deplete (hence its name) the conductive channel of its free electrons switching the transistor “OFF”. Likewise for a p-channel depletion MOS transistor a positive gate-source voltage, +VGS will deplete the channel of its free holes turning it “OFF”.

In other words, for an n-channel depletion mode MOSFET: +VGS means more electrons and more current. While a -VGS means less electrons and less current. The opposite is also true for the p-channel types. Then the depletion mode MOSFET is equivalent to a “normally-closed” switch.

**Depletion-mode N-Channel MOSFET and circuit Symbols**





The depletion-mode MOSFET is constructed in a similar way to their JFET transistor counterparts were the drain-source channel is inherently conductive with the electrons and holes already present within the n-type or p-type channel. This doping of the channel produces a conducting path of low resistance between the Drain and Source with zero Gate bias.

**Enhancement-mode MOSFET**

The more common **Enhancement-mode MOSFET** or eMOSFET, is the reverse of the depletion-mode type. Here the conducting channel is lightly doped or even undoped making it non-conductive. This results in the device being normally “OFF” (non-conducting) when the gate bias voltage, VGS is equal to zero. The circuit symbol shown above for an enhancement MOS transistor uses a broken channel line to signify a normally open non-conducting channel.

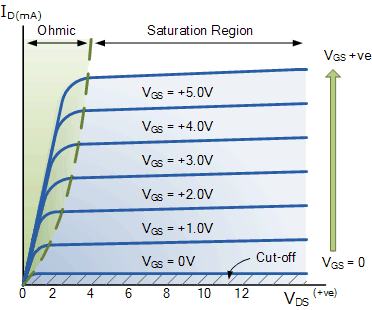
For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage ( VGS ) is applied to the gate terminal greater than the threshold voltage ( VTH ) level in which conductance takes place making it a transconductance device.

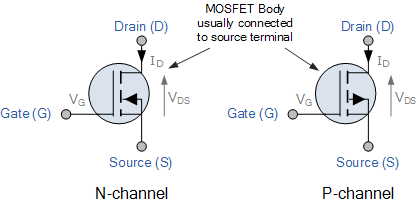
The application of a positive (+ve) gate voltage to a n-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel.

Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current, ID through the channel. In other words, for an n-channel enhancement mode MOSFET: +VGS turns the transistor “ON”, while a zero or -VGS turns the transistor “OFF”. Thus the enhancement-mode MOSFET is equivalent to a “normally-open” switch.

The reverse is true for the p-channel enhancement MOS transistor. When VGS = 0 the device is “OFF” and the channel is open. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it “ON”. Then for an p-channel enhancement mode MOSFET: +VGS turns the transistor “OFF”, while -VGS turns the transistor “ON”.

**Enhancement-mode N-Channel MOSFET and Circuit Symbols**





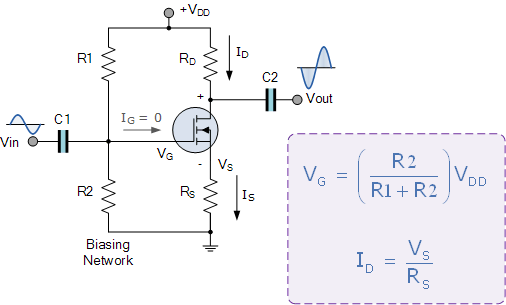
Enhancement-mode MOSFETs make excellent electronics switches due to their low “ON” resistance and extremely high “OFF” resistance as well as their infinitely high input resistance due to their isolated gate. Enhancement-mode MOSFETs are used in integrated circuits to produce CMOS type *Logic Gates* and power switching circuits in the form of as PMOS (P-channel) and NMOS (N-channel) gates. CMOS actually stands for *Complementary MOS* meaning that the logic device has both PMOS and NMOS within its design.

**The MOSFET Amplifier**

Just like the previous Junction Field Effect transistor, MOSFETs can be used to make single stage class “A” amplifier circuits with the enhancement mode n-channel MOSFET common source amplifier being the most popular circuit. Depletion mode MOSFET amplifiers are very similar to the JFET amplifiers, except that the MOSFET has a much higher input impedance.

This high input impedance is controlled by the gate biasing resistive network formed by R1 and R2. Also, the output signal for the enhancement mode common source MOSFET amplifier is inverted because when VG is low the transistor is switched “OFF” and VD (Vout) is high. When VG is high the transistor is switched “ON” and VD (Vout) is low as shown.

**Enhancement-mode N-Channel MOSFET Amplifier**



The DC biasing of this common source (CS) MOSFET amplifier circuit is virtually identical to the JFET amplifier. The MOSFET circuit is biased in class A mode by the voltage divider network formed by resistors R1 and R2. The AC input resistance is given as RIN = RG = 1MΩ.

Metal Oxide Semiconductor Field Effect Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage.

The MOSFETs ability to change between these two states enables it to have two basic functions: “switching” (digital electronics) or “amplification” (analogue electronics). Then MOSFETs have the ability to operate within three different regions:

* 1. Cut-off Region   –   with VGS < Vthreshold the gate-source voltage is much lower than the transistors threshold voltage so the MOSFET transistor is switched “fully-OFF” thus, ID = 0, with the transistor acting like an open switch regardless of the value of VDS.
* 2. Linear (Ohmic) Region   –   with VGS > Vthreshold and VDS < VGS the transistor is in its constant resistance region behaving as a voltage-controlled resistance whose resistive value is determined by the gate voltage, VGS level.
* 3. Saturation Region   –   with VGS > Vthreshold and VDS > VGS the transistor is in its constant current region and is therefore “fully-ON”. The Drain current ID = Maximum with the transistor acting as a closed switch.

**MOSFET Tutorial Summary**

The Metal Oxide Semiconductor Field Effect Transistor, or **MOSFET** for short, has an extremely high input gate resistance with the current flowing through the channel between the source and drain being controlled by the gate voltage. Because of this high input impedance and gain, MOSFETs can be easily damaged by static electricity if not carefully protected or handled.

**MOSFET’s** are ideal for use as electronic switches or as common-source amplifiers as their power consumption is very small. Typical applications for metal oxide semiconductor field effect transistors are in Microprocessors, Memories, Calculators and Logic CMOS Gates etc.

Also, notice that a dotted or broken line within the symbol indicates a normally “OFF” enhancement type showing that “NO” current can flow through the channel when zero gate-source voltage VGS is applied.

A continuous unbroken line within the symbol indicates a normally “ON” Depletion type showing that current “CAN” flow through the channel with zero gate voltage. For p-channel types the symbols are exactly the same for both types except that the arrow points outwards. This can be summarised in the following switching table.

|  |  |  |  |
| --- | --- | --- | --- |
| MOSFET type | VGS = +ve | VGS = 0 | VGS = -ve |
| N-Channel Depletion | ON | ON | OFF |
| N-Channel Enhancement | ON | OFF | OFF |
| P-Channel Depletion | OFF | ON | ON |
| P-Channel Enhancement | OFF | OFF | ON |

So for n-type enhancement type MOSFETs, a positive gate voltage turns “ON” the transistor and with zero gate voltage, the transistor will be “OFF”. For a p-channel enhancement type MOSFET, a negative gate voltage will turn “ON” the transistor and with zero gate voltage, the transistor will be “OFF”. The voltage point at which the MOSFET starts to pass current through the channel is determined by the threshold voltage VTH of the device.

In the next tutorial about **Field Effect Transistors** instead of using the transistor as an amplifying device, we will look at the operation of the transistor in its saturation and cut-off regions when used as a solid-state switch. Field effect transistor switches are used in many applications to switch a DC current “ON” or “OFF” such as LED’s which require only a few milliamps at low DC voltages, or motors which require higher currents at higher voltages.