

Diode Clamping Circuits

Basic Definition:

The clamping circuit (*clammer*) is one will "clamp" a signal to a different dc level. The circuit must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval ($T/2$) the diode is non-conducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants. Therefore, the condition required for the capacitor to hold its voltage during the discharge period between pulses of the input signal is

$$5\tau = 5RC \gg \frac{T}{2} = \frac{1}{2f}$$

Example -1:

Determine the output (v_o) for the circuit of Fig. -1 for the input (v_i) shown.

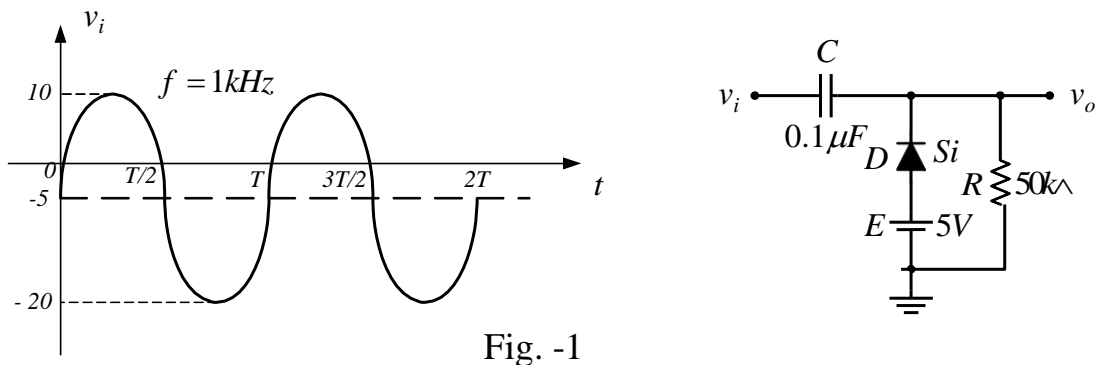


Fig. -1

Solution:

The analysis of clamping circuits are started by considering that the part of the input signal that will forward bias the diode. For the circuit of Fig. -1, the diode is forward bias ("on" state) during the negative half period of the input signal (v_i) and the capacitor will charge up instantaneously to a voltage level determined by the circuit of Fig. -2.

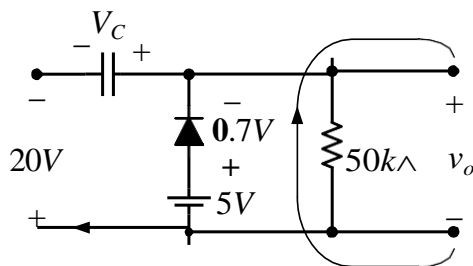


Fig. -2

For the input section KVL will result in

$$-20 + V_C + 0.7 - 5 = 0 \Rightarrow V_C = 24.3 \text{ V.}$$

The output voltage (v_o) can be determined by KVL in the output section

$$+5 - 0.7 - v_o = 0 \Rightarrow v_o = 4.3 \text{ V.}$$

Now check that the capacitor will hold on or not its establish voltage level during the period (positive half period in case of Example -1) when the diode is in the "off" state (reverse bias). The total time constant 5τ of the discharging circuit of Fig. -3 is determined by the product $5RC$ and has the magnitude

$$5\tau = 5RC = 5 (50 \times 10^3) (0.1 \times 10^{-6}) = 25 \text{ ms.}$$

The frequency (f) is 1 kHz, resulting in a period of 1 ms and an interval of 0.5 ms between levels, that is

$$T/2 = 1/(2f) = 1/(2 \times 1 \times 10^3) = 0.5 \text{ ms.}$$

We find that

$$5\tau \gg T/2 \text{ (} 25\text{ms} / 0.5\text{ms} = 50 \text{ times).}$$

So that, it is certainly a good approximation that the capacitor will hold its voltage (24.3 V) during the discharge period between pulses of the input signal.

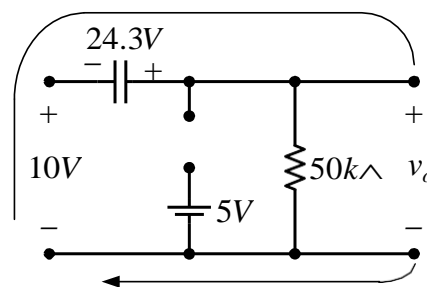


Fig. -3

The open-circuit equivalent for the diode will remove the 5-V battery from having any effect on v_o , and applying KVL around the outside loop of circuit will result in

$$+10 + 24.3 - v_o = 0 \Rightarrow v_o = 34.3 \text{ V.}$$

The resulting output appears in Fig. -4, where the input and the output swing are the same.

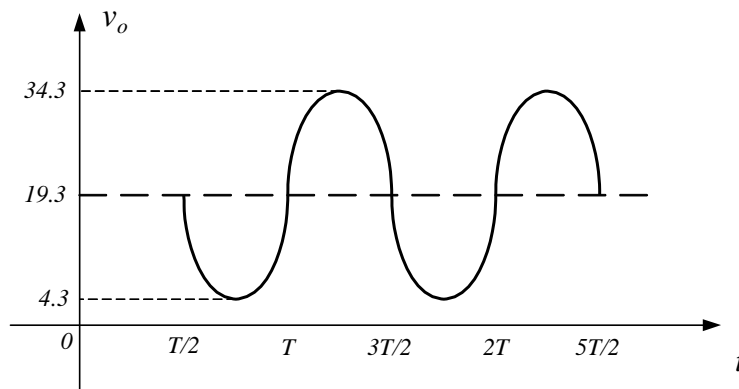


Fig. -4

Example -2:

Determine the output (v_o) for the circuit of Fig. -5 for the input (v_i) shown

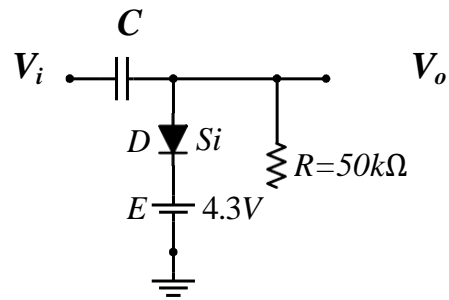
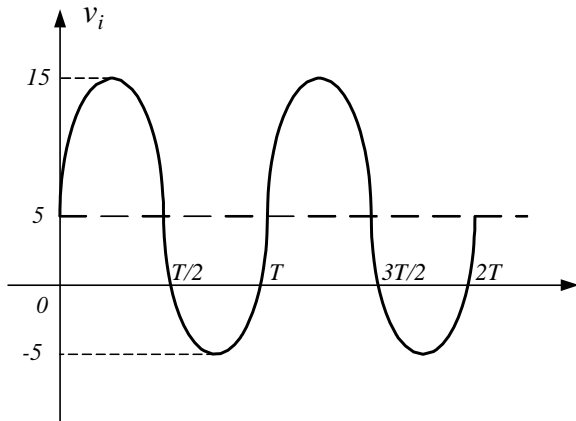


Fig. -5

Solution:

The output voltage (v_o) can be determined by KVL in the output section shown in Fig. -5.

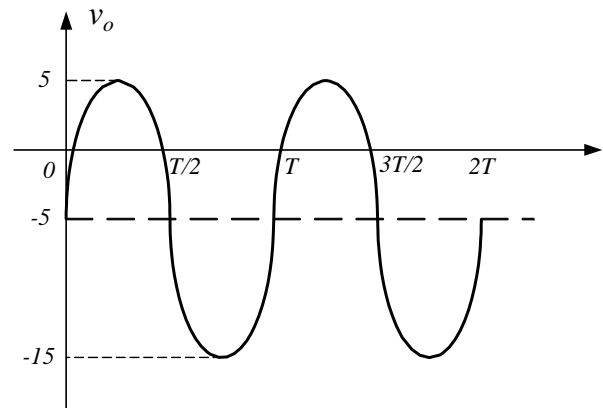
$$4.3 + 0.7 - v_o = 0 \Rightarrow v_o = 5 \text{ V.}$$

For the input section KVL will result

$$15 + V_C - 5 = 0 \Rightarrow V_C = -10 \text{ V.}$$

The open-circuit equivalent for the diode will remove the 4.V battery from having any effect on v_o , and applying KVL around the outside loop of circuit will result in

$$-5 -10 + v_o = 0 \Rightarrow v_o = -15 \text{ V.}$$



The output signal is shown in Fig-6.

EXAMPLE 3. Determine v_o for the network of Fig. -7 for the input indicated.

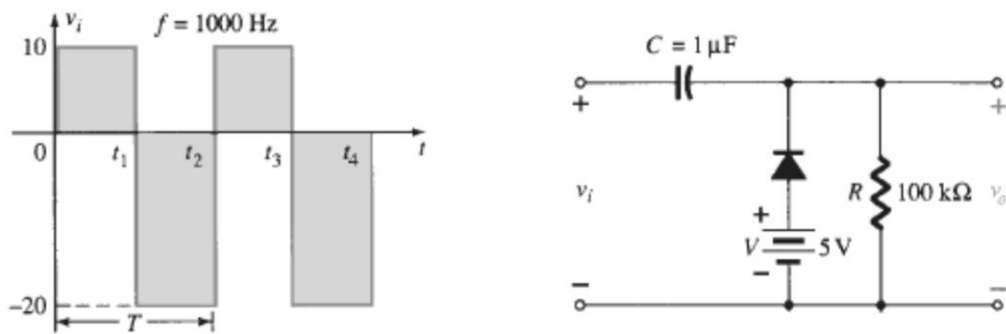
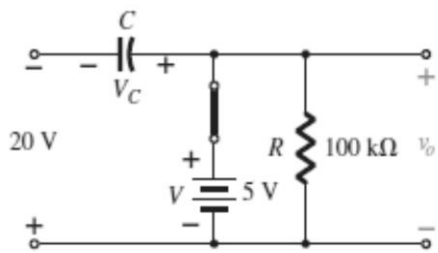
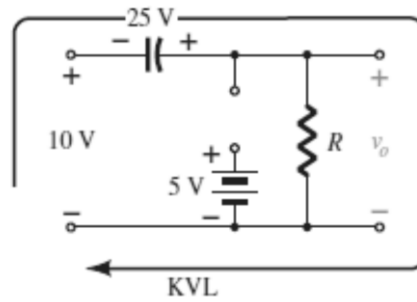


Fig. -7

Solution:



$$\begin{aligned}
 -20 \text{ V} + V_C - 5 \text{ V} &= 0 \\
 \text{and } V_C &= 25 \text{ V} \\
 +5 - v_o &= 0 \\
 \text{and } v_o &= 5 \text{ V}
 \end{aligned}$$



$$\begin{aligned}
 +10 \text{ V} + 25 \text{ V} - v_o &= 0 \\
 \text{and } v_o &= 35 \text{ V}
 \end{aligned}$$

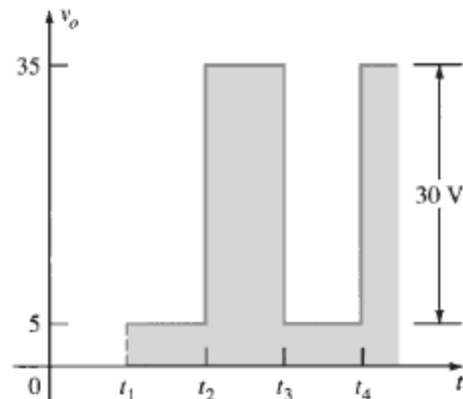
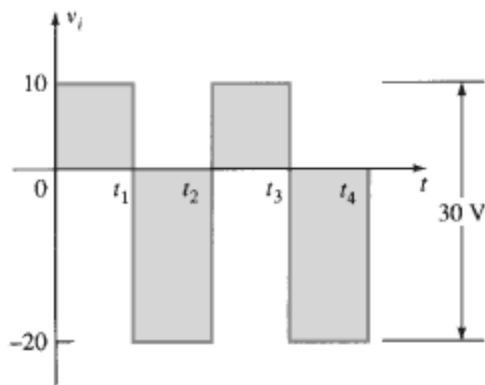
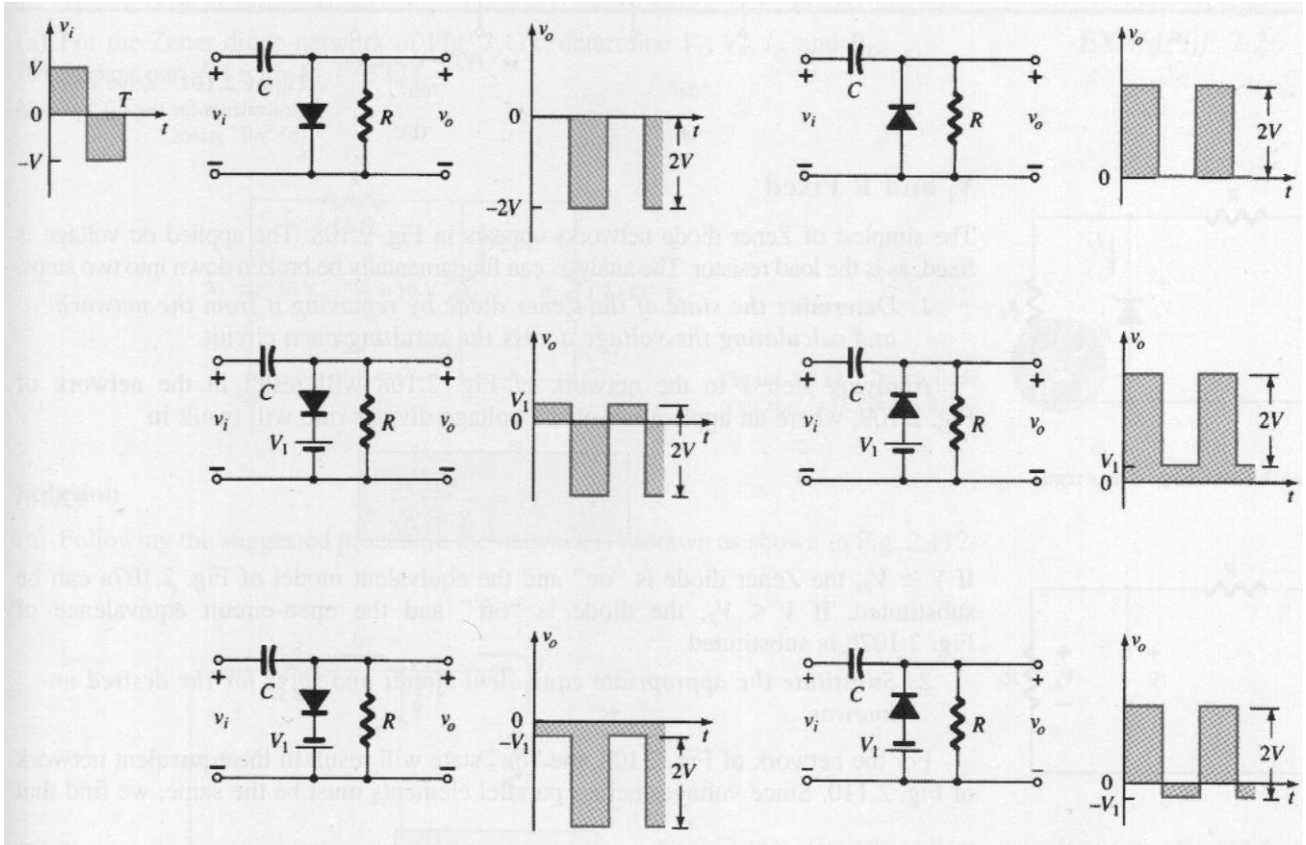


Fig-8



Clampers with ideal diodes and $5\tau = 5RC \gg T/2$

Fig. -9

